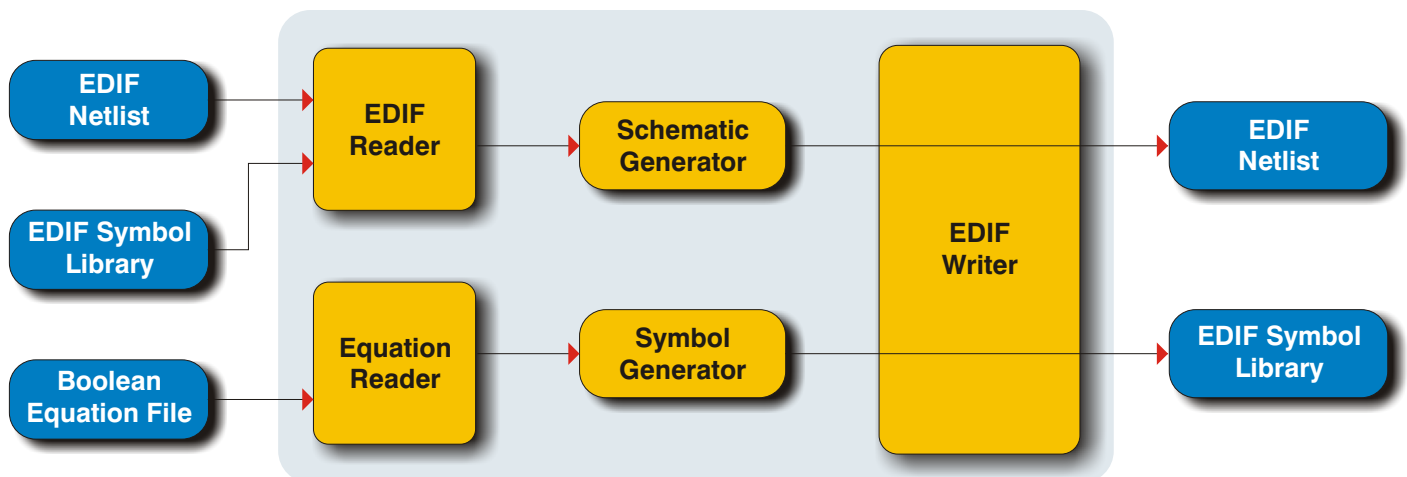


EDIF Netlist to Schematic Convertor - N2S

This tool generates EDIF schematics from EDIF netlists. The schematics generated by this tool can be used by schematic viewers and editors to provide designers with an intuitive interface to design descriptions. It employs aesthetic algorithms for Place and Route to mimic the manually generated schematics.

Key Features

- ▶ Accepts EDIF 200 netlist descriptions as input and generates schematics in EDIF 200 format. Symbol information can be specified through EDIF 200 symbol libraries
- ▶ Generates regular, symmetrical schematics that are close to hand generated schematics
- ▶ Generates black-box symbols for components that do not have symbol specified
- ▶ Generates meaningful symbols for components from boolean equations that describe their functionality
- ▶ Automatically partitions the schematic diagram into pages of user-defined dimensions
- ▶ Can handle hierarchical netlists and generates the hierarchical schematics
- ▶ Available on Solaris 2.5.1 onwards and HP-UX 9.05



Key Components

- EDIF Reader parses the input EDIF netlist description and EDIF symbol library, if specified, and populates internal abstract netlist representation used by subsequent modules.
- Equation Reader parses the input Boolean equation file and generates an internal representation for equations of each component specified in the file. After that, for each component, the module generates an abstract netlist representation consisting purely of primitive gates that implements the component's equation.
- Schematic generator performs schematic layout on the abstract netlist representation and generates the schematic information for the circuit. The internal data structures are updated with this schematic information.
- Symbol Generator operates on the abstract representation created by the Equation Reader and generates a symbol for it. The symbol, when finally viewed on a schematic, would make the functionality of that particular component very evident to the user.
- EDIF Writer traverses the internal netlist representations and generates EDIF descriptions for them. Depending upon whether the EDIF Writer is working on data from the Schematic generator or the Symbol Generator, it generates either an EDIF schematic or an EDIF symbol library.