

VERILOG FRONT END

Introduction

SoftJin offers re-usable proven EDA components to its customers with full source code licensing. SoftJin can also customize these components and integrate them with your existing tools. SoftJin's EDA components provide the customers with robustness of proven performance along with the flexibility of customization.

Verilog Front End

This is a front-end tool for the IEEE Verilog Hardware Description Language. It parses the input Verilog description and populates an in-core representation of the input.

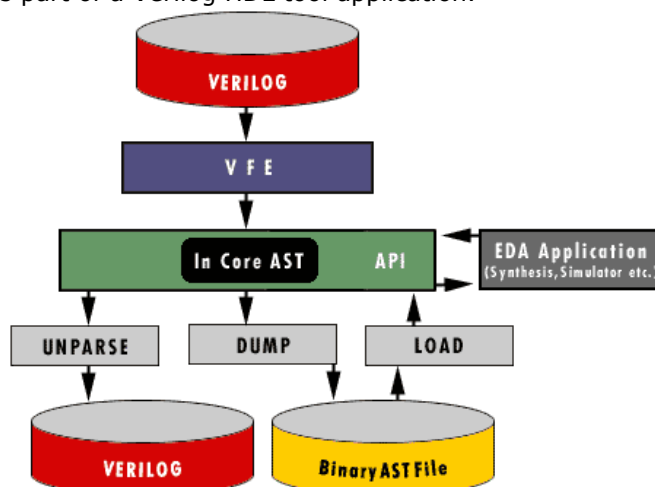
The Verilog front-end (VFE) tool is a useful building block for the in-house design automation groups of electronic design companies as well as the EDA companies developing Verilog based Synthesis, Verification and other tools.

Advantages of SoftJin's Verilog Front End Tool

- Extremely fast processing for large designs (both RTL and netlists)
- Compact Abstract Syntax Tree database allows space efficient handling of very large designs
- Rich set of API functions help easy integration and quick development
- Stable and tested software, being used by over 2000 designers in a large Japanese semiconductor company.

Architecture

The flowchart that follows illustrates a typical usage of VFE as part of a Verilog HDL tool application.



The following are the key features of the Verilog HDL Front End.

Complete Language Support

- Compliant with IEEE 1364 Verilog standard
- Supports behavioral, RTL and netlist description
- Supports parameterized design
- Supports UDP, specify block parsing

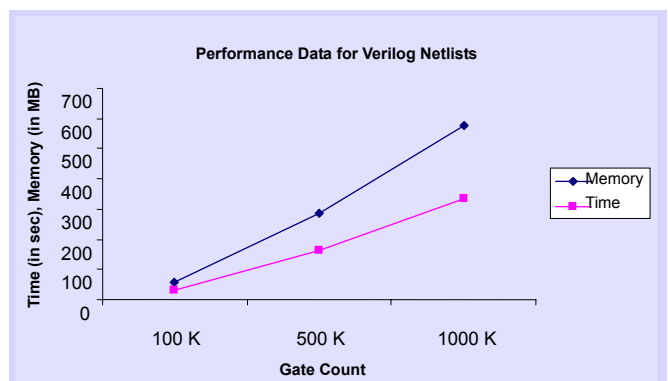
Processing

- Performs detailed syntax and semantic analysis
- Creates in-core Abstract syntax tree (AST) data structure
- Close association with Verilog code and nodes in AST through file name, line/column number
- Intuitive C-like API functions to access/modify nodes of AST
- Retains user specified comments in comments-database
- Support for translate on/off directive for conditional parsing
- Facility to generate Verilog code back from the AST
- Binary dump/load of the AST on/from disk

Performance Data

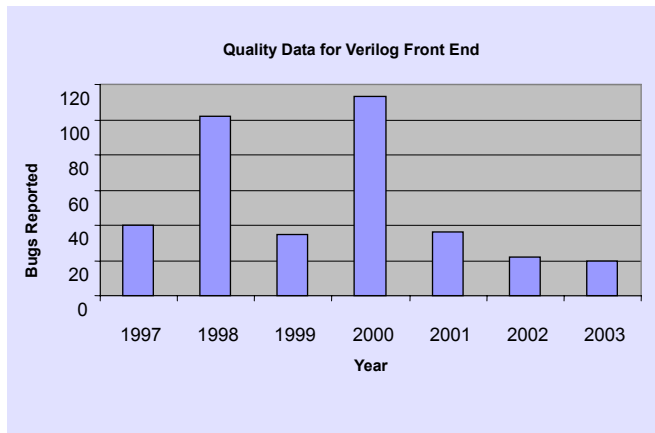
Currently, this tool is being used by over 2000 designers in the customer organization as part of various HDL based tools.

The Verilog Front-end (Parser Component) has been extensively used and evaluated. This section gives performance data on some examples. The following data has been computed on Sun Enterprise 450 (4 X UltraSPARC II 480 MHz) machine, with 4 GB RAM, and 5.2 GB SWAP.



As it can be observed from the above data, the performance is linear in size of design descriptions, both for RTL and netlist descriptions.

HDL Front End has been tested extensively on million gate designs for performance. A feature-wise test bench was used for completeness in testing



The test results are an indication of the quality and stability of the software.

Multiple Platform Support

- Sun Solaris 2.6 onwards
- Linux
- Windows NT 4.0

Customization Services

- We can customize the Verilog front-end for your requirements. For example, the front-end can be enhanced to include:
 - ▶ SystemVerilog support
 - ▶ Hierarchy flattening
- We can develop customer specific HDL tools on top of the Verilog Front-End.

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