

Programmable Synthesis Engine

Customizable Logic Synthesis Engine for FPGAs and Programmable Fabrics

SoftJin's Programmable Synthesis Engine (PSE) is a Logic Synthesis engine that is customizable for a variety of programmable platform architectures, such as Look-up Table (LUT) and other configurable logic architectures.

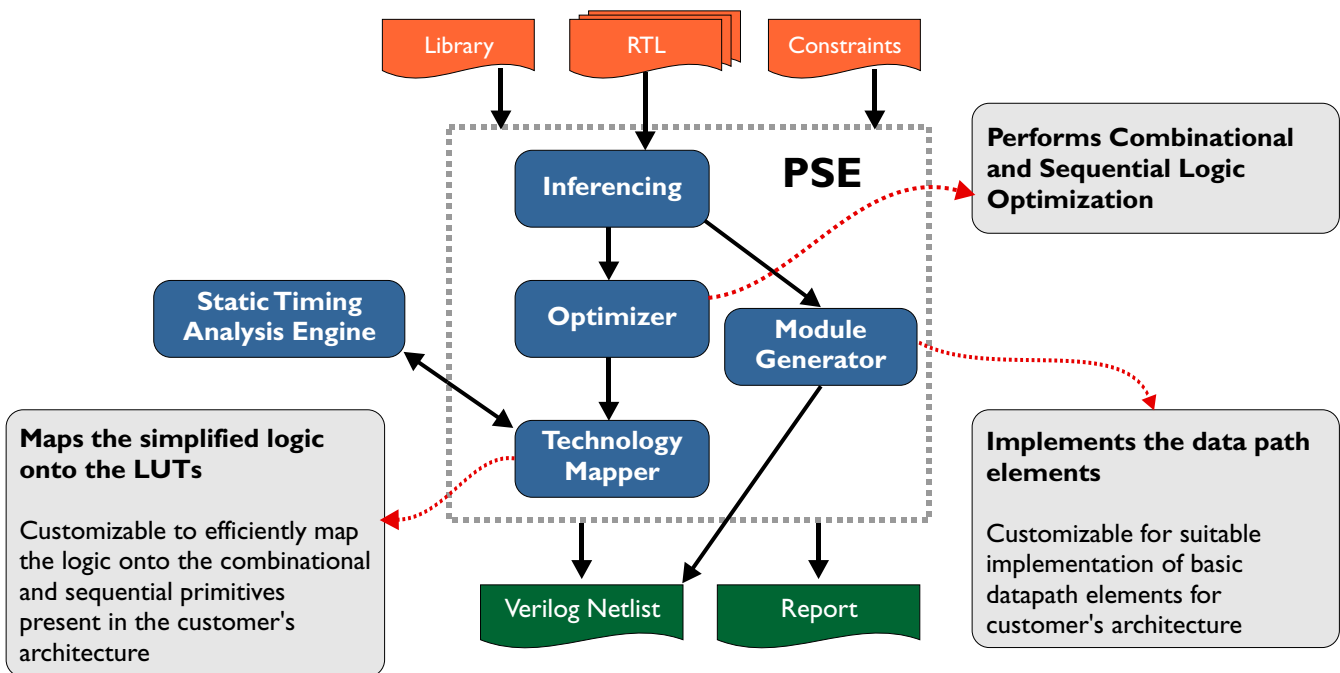
SoftJin's PSE is a core EDA component that can be used by vendors of Programmable Platforms such as FPGAs, Structured ASIC and other innovative programmable fabrics to offer a customized Logic Design Tool to their users. SoftJin customizes PSE to specific programmable platform architecture and for integration with placement and routing tools. Easy customizability of PSE's underlying Optimization, Module Generation and Technology Mapping components enables Programmable Platform vendors to offer a Logic Synthesis Solution that derives the best out of the underlying architecture and deliver much improved QoR (Quality of Results) as compared to superficially customized versions of standard off-the-shelf FPGA/ASIC Synthesis tools.

PSE can also be licensed by System-level EDA companies who would like to extend their offerings into the RTL domain. For example, for Behavioral synthesis tool vendors, that are targeting programmable platforms such as FPGAs, rather than stopping at RTL output, integrating PSE into their solution offers a platform neutral approach all the way to Netlist.

PSE accepts RTL HDL, performs a host of technology independent and technology dependent optimizations. It then performs an architecture specific mapping to generate a delay and area optimal implementation of the design for the targeted programmable platform.

Key Benefits for Programmable Fabric Vendors

- **Optimized Logic Synthesis Solution -** PSE based Logic Synthesis Solution takes full advantage of specific data-path elements, custom IP blocks and random logic available in your target architectures. This enables you to provide better QoR to your users as compared to standard ASIC/FPGA Logic Synthesis tools.
- **Lower cost of ownership -** A combination of PSE licensing and customization offers much lesser cost of ownership as compared to developing such a solution in-house or licensing it from standard off-the-shelf EDA vendor. This allows you to offer an affordable yet efficient Synthesis tool to your users.
- **Host of in-built optimizations and support for high level primitives -** PSE has a host of built-in high level and technology independent optimizations. Also, PSE's module generator recognizes and maps a variety and growing list of higher level primitives such as arithmetic operators to the available datapath element of the architecture.



Key Features

Inferencing

PSE analyzes input description in detail to identify the circuit components so that the mapping can be done most effectively. The basic components it identifies include:

- Combinational circuit portion
- Sequential components
- Memories RAMs/ROMs
- Finite State Machines
- Arithmetic Functional Units like Adder, Multiplier etc.
- Inputs-Outputs

Technology Independent Optimizations

PSE has a host of Technology Independent optimizations at the RTL and the combinational logic level to reduce the design size and improve design performance. These include:

- Tree height reduction
- Constant and Variable propagation
- Common subexpression elimination
- Dead code elimination
- Operator strength reduction
- Boolean Logic Optimizations

Technology Mapping

PSE's technology mapper implements the optimized abstract logic and the abstract sequential elements present in the input onto target technology in an efficient manner such that the resources on the target device are effectively

used in conjunction with minimum delay. Within the overall constraint of optimizing the solution for minimum delay by driving the Mapper in a timing-driven mode, it optimizes the design for minimum area.

- Supports heterogeneous LUT mapping 3 input to 8 input LUTs. Useful for architecture exploration
- Carry Chain Mapping for efficient realization of fast adders, counters, multipliers etc.
- Maps sequential logic to DFF with enable & set/reset
- Maps I/O pin onto technology input/output buffer
- Maps three-state logic onto technology specific tri-state buffer, if available
- Maps onto DDR I/O Pads, if available

PSE can be integrated with SoftJin's Static Timing Analysis Engine library to offer a Timing driven Synthesis Solution.

Architecture Specific Module Generator

PSE's module generator recognizes and maps a variety and growing list of higher level primitives such as arithmetic operators to the available datapath elements of the architecture such as:

- Addition/ subtraction
- Multiplication/ Division
- Compare
- Shift, rotate
- Decoder, MUX

PSE Customization and Integration Services

PSE has been regression tested on thousands of designs. For verification purposes, it is also integrated with various Functional Verification tools including Formal Verification tools. Along with PSE, SoftJin offers PSE's customization and integration services, whereby SoftJin takes the responsibility of customizing PSE for programmable platform vendor's architecture and integrating PSE with the other tools in the design flow.



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