

SoftJin's Design Technology Services

SoftJin offers the following services as part of its Design technology offering:

- ▶ Design Methodology development
- ▶ Optimization of Quality of Results
- ▶ Qualification of new design flows
- ▶ Design Infrastructure development

Design Technology – The challenges

Leading semiconductor design companies follow structured and unique design methodologies that imbibe best practices

Such leading design teams are faced with challenges of nanometer design namely:

- ▶ Nanometer Design Flows and tools are in constant evolution
 - System Level Design complexity
 - Interoperability issues within single or multiple EDA vendors' flow
 - Gaps in traditional IC Design methodology
- ▶ Multiple EDA Methodology requirements across various teams in the same organization.
- ▶ EDA group's challenge magnified from Maintenance and Enhancement of EDA tools to creating and maintaining EDA Methodology

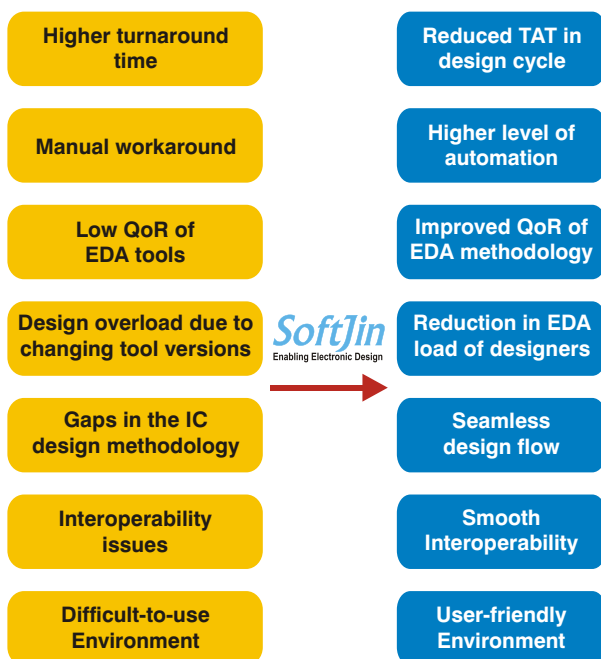
Why SoftJin?

SoftJin, with its unique EDA software development services as well as vendor-neutral background, is a natural choice for helping you in tackling these design flow challenges:

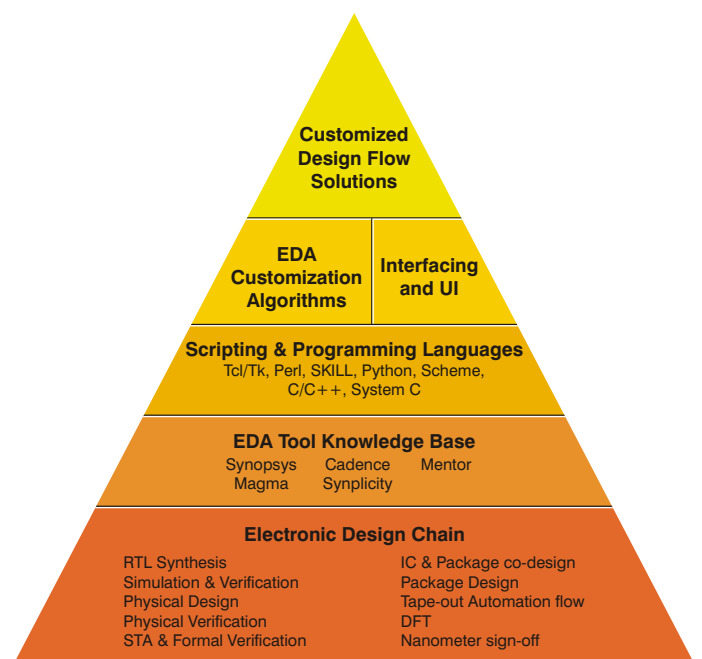
- A strong background in EDA tools development gives us the real insight into the functionality of tools which goes beyond the tool knowledge to an algorithmic level
- We have expertise spread across the design spectrum and across EDA products from various vendors.
- A versatile team consisting of people with extensive design, application engineering as well as software development background

- Our strong project management and services delivery process honed by years of working with large-scale EDA software development projects and working with leading design teams worldwide

SoftJin Design Technology services - Benefits



SoftJin Skill Pyramid



SoftJin's Experience

SoftJin has significant experience in delivering design technology services:

Design methodology development

SoftJin has developed design flow and methodology for a new wafer-level integration manufacturing technology of our client. Existing EDA tools and flows did not address the issues for this technology.

SoftJin set up an optimal physical design flow with existing EDA tools of Monterey [Dolphin/Sonar, MTC] and Synopsys [Power Compiler] and developed a minimum set of new customized EDA tools to derive the key advantages of the new technology

FPGA Verification methodology development

SoftJin has developed a SystemC based verification methodology that reduces overall verification time in the front-end design flow. The cornerstone of this approach is in the usage of SystemC testbenches for verifying designs at the unit level as well as the system level.

Nanometer Sign-off flow

SoftJin is involved in validation a sign-off flow using tools from a new vendor. This project involves establishing and comparing the Quality of Results [QoR] from the new flow with the previous sign-off flow, as well development of scripts to enable seamless usage of the new design flow by design engineers. The sign-off tools include Power Integrity and Signal Integrity tools.

Cell characterization flow

In this project, SoftJin developed an engine that automated and validated inputs to the cell characterization flow of the customer. This enabled data completeness and consistency for the cell characterization flow. The engine guides the user to give correct inputs required for characterization. This engine was a configurable Perl-based engine which performs completeness and consistency checks. The outputs generated by this Cell characterization flow are validated using Synopsys Library Compiler.

Development of Parameterized Cells for Analog Layout automation

Reduction of Analog design cycle time is getting critical with new emerging technologies. The P-Cell library concept is meant to reduce design cycle time and provides reduction of :

1. Layout design time
2. Migration time from one technology node to the other
3. Verification overhead to layout designer.

SoftJin was involved in

1. Developing various generic cell definitions which would then be used by a particular technology to generate layouts using Cadence SKILL language.
2. Developing DRC/LVS/LVL clean - technology specific wrappers and cells, using Cadence OPUS II.
3. Developing UI to facilitate technology specific cells generation from Virtuoso Layout Editor.

Table I : SoftJin skills in Commercial EDA tools

Cadence	Magma	Mentor	Synopsys	Other
<ul style="list-style-type: none"> ▶ SoC Encounter ▶ Virtuoso Environment ▶ Voltage Storm ▶ CeltIC ▶ Allegro Package Designer ▶ Assura ▶ Diva ▶ Dracula ▶ Fire & Ice 	<ul style="list-style-type: none"> ▶ BlastFusion 	<ul style="list-style-type: none"> ▶ Calibre ▶ Fastscan ▶ Flextext ▶ DFT Advisor ▶ MBIST Architect ▶ IC Station 	<ul style="list-style-type: none"> ▶ Astro ▶ Astro-Rail ▶ Physical Compiler ▶ Design Compiler ▶ PrimeTime ▶ PrimeTime - SI ▶ Hercules ▶ Star RCXT ▶ PowerCompiler ▶ Jupiter XT ▶ PathMill ▶ HSpice 	<ul style="list-style-type: none"> ▶ FPGA Tools ▶ Various Internal tools of customers



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