

SYSTEM SOFTWARE AND HARDWARE DEVELOPMENT FOR IC PACKAGING EQUIPMENT

Customer

This case study describes SoftJin's engagement with IC Packaging Equipment Vendor and its customer (a leading Japanese IC Packaging vendor) for the development of a Maskless Exposure System for PCB and IC package manufacturing.

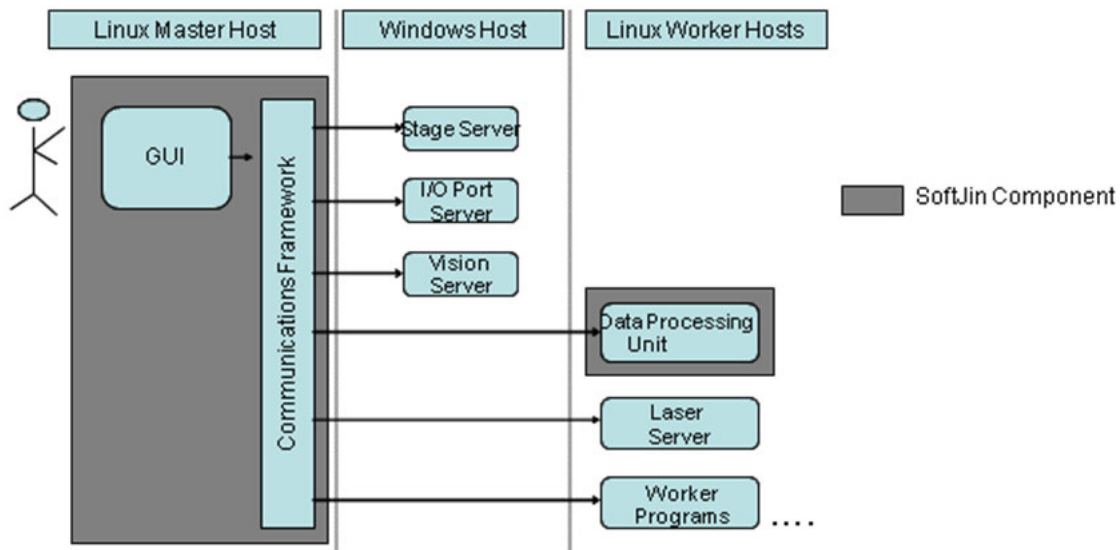
Project Overview

To support their advanced technology, the equipment vendor has developed a Maskless Exposure System for production of high resolution Printed Circuit Boards (PCB), display panels, and high-density chip packaging. SoftJin has developed key system components (Figure 1) of this system.

SoftJin's role in the system is as follows:

- Research and Develop key computationally intensive real-time geometrical data processing software components for the exposure equipment to be used in production environment.
- SoftJin also developed the Front End Graphical User Interface (GUI) for the Maskless Exposure System, so that the operator gets an integrated view of the whole system for process control. The operator is presented with a Graphical User Interface (GUI), which can be used to view and control various operations of the system.
- Implement multi-FPGA based hardware for speeding up computationally intensive tasks.

Figure 1: Maskless Exposure System Components



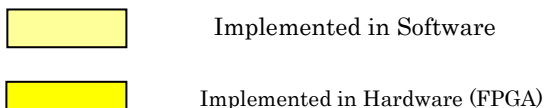
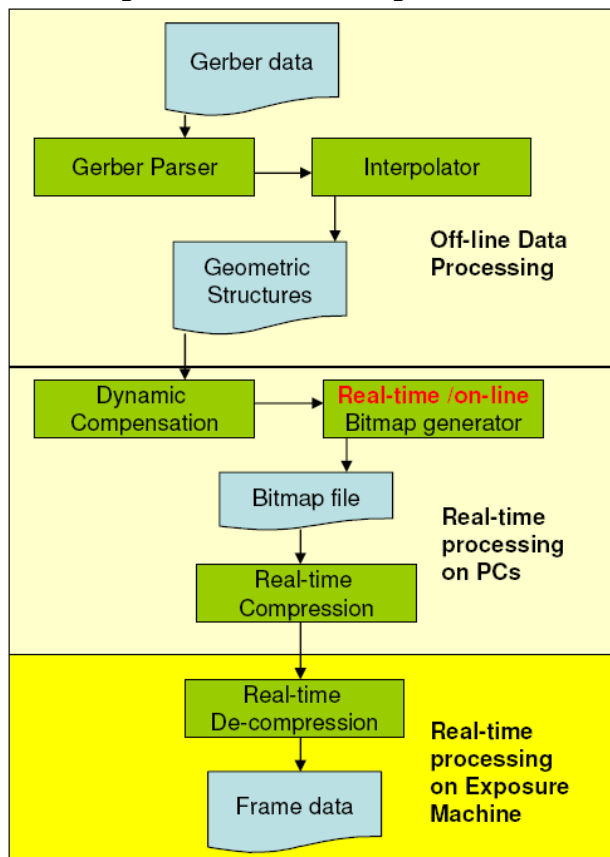
SoftJin Impact on the Project

- SoftJin's dynamic data compensation and compression algorithms used in the Data Preparation Stage resulted in substantial improvement in data communication speed and overall machine throughput.
- SoftJin's multi-FPGA, pipelined architecture design resulted in 2X improvement in speed of real-time data processing.
- Multi-year software and hardware engagement resulted in customer exceeding its performance targets from Data-processing System and successfully deploying the system in 2006.

Data Processing System

The input accepted by the Maskless Exposure System is the Industry standard Gerber format, which is a description format for package layout data. The data preparation process involved in converting the layout data using geometric operations into an intermediate format is shown in Figure 2. This intermediate format would later be converted into a bitmap format accepted by the Maskless exposure system. In real time environment, the bitmap format needs to be compressed to send through the slow physical channel and again to be decompressed at the machine end. Also data needs to be compensated in real time due to mechanical and environmental fluctuations.

Figure 2: Data Processing Unit



Software Sub-system

Data preparation involves various software components developed by SoftJin, as shown in Figure 2. Key components and features of the software sub-system are:

- A *Gerber Parser*, developed by SoftJin, which supported the recommended usage of the format. Most of the Gerber Parsers available make very simplistic assumptions while carrying out *geometric interpolations* for ease in implementation. However, SoftJin's Gerber parser makes no such assumptions and truly represents the Gerber specifications.
- Convert Gerber data into polygonal geometric data structures. This involves the following:
 - Carry out Boolean and sizing operations
 - Use of Distributed processing
- Apply real time compensations for translation, rotation and warping on the geometric data
- Convert compensated geometric data into Equipment defined interleaved bit map format
- Transfer the bitmap data to exposure equipment in customized compressed form
- Decompress the compressed bitmap data in the exposure equipment side
- Convert the interleaved bitmap data into frame data as required by exposure machine
- Off-line and on-line validation (full layout as well as random sampling) of generated data (vector, bitmap, frame data)

Key Performance Metric achieved

Real-time, dynamic compensation and data compression/de-compression techniques enabled 20X speed-up in data communication between PC and System, thus significantly impacting the overall System throughput.

FPGA based Hardware Sub-system

SoftJin has implemented the real time processing Unit in machine in board using multiple FPGAs (Figure 3). The functionalities include

- Decompress the compressed bitmap data in the exposure equipment side
- Convert the interleaved bitmap data into frame data as required by exposure machine

In this process SoftJin's contributions are

- Realization of hardware using multiple FPGAs. Multiple memories used as buffers for each stage of macro-pipeline FPGA system.
- Integration of FPGA devices with Board
- Achieved desired overall throughput of the system – data driven to lithography equipment at 1 GigaBytes/sec

The key FPGA design related skills used in these projects are:

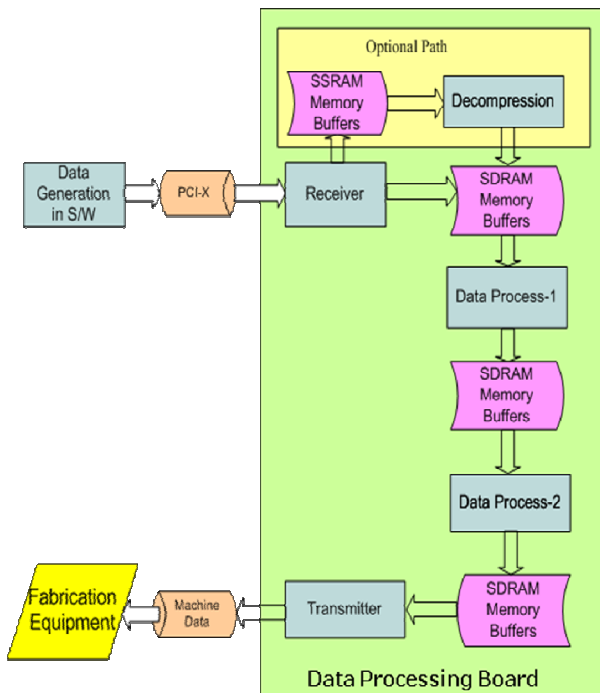
System level design

- Hardware-Software Partitioning
- Hardware - Software Co-Verification using SystemC
- Multi-FPGA Partitioning

FPGA Implementation

- RTL modeling using Verilog, VHDL
- Platform FPGA design using Xilinx Virtex Pro
- Usage of standard design elements including DDR SDRAM memory controller, Bus Controller
- Tools used - Synplify Pro, Xilinx XST, ModelSim with SystemC

Figure 3: Real Time Processing Unit on Exposure Machine



Key Features

- High speed and pipelined Data Processing Stages on Data Processing Board (DPB)
- Multiple memories used as buffers for each stage for macro-pipelining
- SDRAM memories working in DDR mode on 133 MHz clock
- High Speed transmission of data to the Fabrication Equipment (1 GBytes/sec)
- Four Virtex-II Pro (XC2VP70/FF1704) FPGAs, Five 512 MB DDR SDRAM (133 MHz) memories, Two 2 MB Pipelined DCT SSRAM memories.

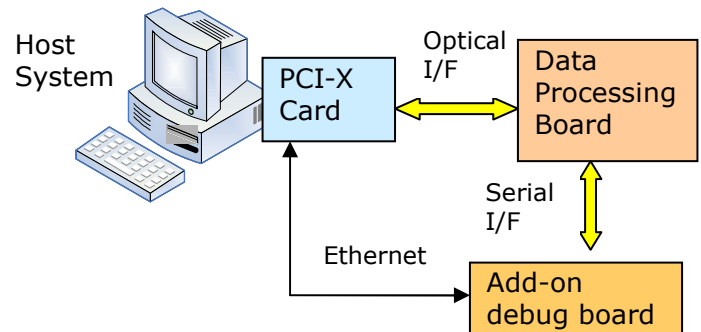
Key Performance Metric Achieved

2X improvement of the speed of real time data processing system due to pipelined architecture.

Hardware Software Sub-System Integration

SoftJin has also implemented the interface between the software sub-system (running on PC) and the FPGA based hardware system to develop the complete data processing unit

Figure 4: Integration of hardware and software sub-systems



- Serial Interface to an Add-on board for real-time debugging
- High speed optical interface board to fetch data from workstation using PCI-X
- DDR interface with manufacturing equipment

Verification Methods

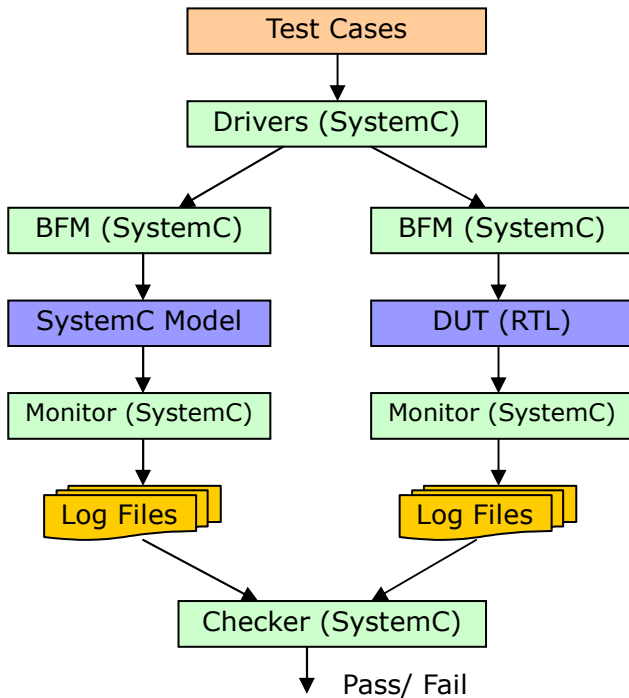
SoftJin has used several verification strategies for verify the functional as well as timing correctness of the hardware sub-system developed. Some of these verification strategies are

SystemC based Verification Strategy

- Proprietary verification strategy using re-usable SystemC testbenches
- Synthesizable test-bench to allow on-chip verification of RTL module
- Use of SystemC TLM for faster Multi-FPGA Design Simulation

Advantages

- Allows Transaction Level, Cycle-accurate and pin-accurate modeling
- HDL model and SystemC model can be used interchangeably
- Each partition of the system simulated at RTL separately (Remaining system at high level TLMs)



Synthesizable Test Bench based Verification Strategy

- Synthesize DUT as well as Drivers and Checkers onto the FPGA logic
- Using embeddable Processor cores (such as PicoBlaze Microcontroller) to control Verification
- Use embedded RAMs (Block RAMs) to store the test inputs and the expected outputs

Advantages

- Assures functional correctness on actual hardware
- 20X reduction in simulation time

SoftJin's System Development Offerings to Semiconductor Equipment Company

