

ENABLING RTL-TO-GATE EQUIVALENCE CHECKING

- ▶ Fujitsu Labs of America [FLA] accelerated its product development plans by outsourcing development of a key component of its product to SoftJin
- ▶ SoftJin developed an RTL-to-Gate Inferencing capability for FLA
- ▶ The project was executed offshore at SoftJin's development centre at Bangalore

Customer

This case study describes SoftJin's engagement with Fujitsu Labs of America [FLA], a wholly owned subsidiary of Fujitsu Laboratories Ltd., focusing on advanced research in VLSI CAD, Internet related technology and LSI technology.

FLA develops EDA software which is beyond what is available from commercial vendors, based upon results of FLA's VLSI CAD research. These applications are used internally by Fujitsu Ltd., and related companies in Japan.

Project Overview

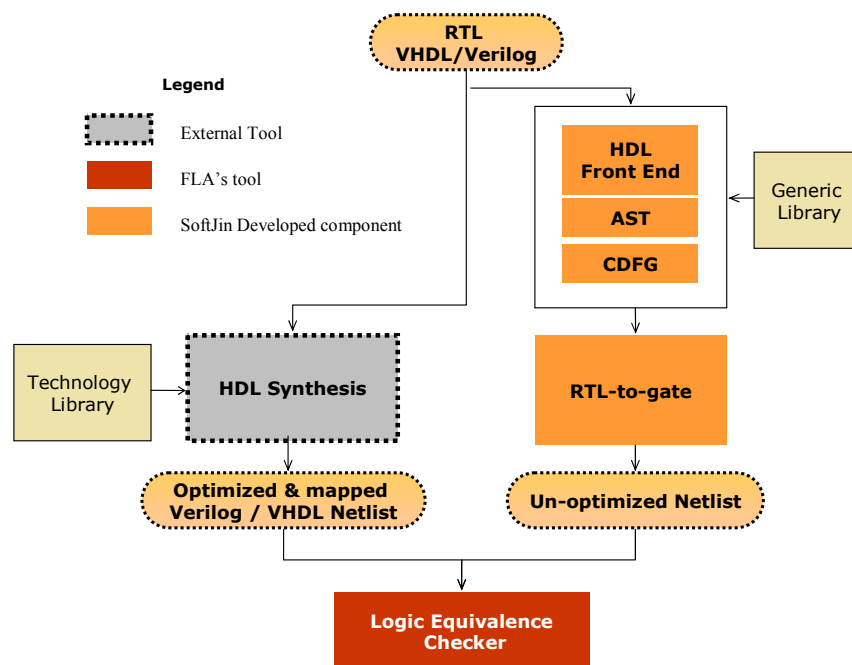
FLA has developed an application for performing formal verification of logic designs. The capability of this tool was "equivalence checks" of gate level design consisting of combinational gates, flip-flops/latches and tri-state buffers. This equivalence checker tool

used Verilog and VHDL readers previously developed by SoftJin.

FLA planned to enhance this tool to include RTL to Gate comparison capabilities. Hence, the HDL Front End had to be enhanced to infer the gate level netlist from the RTL constructs. RTL Inferencing is the process of synthesizing a gate level netlist from an RTL description without any optimizations and mapping to specific technology libraries. Hence, it can be described as a light synthesis tool.

The logic equivalence checker with RTL-to-gate capability helps verification engineers in many ways. Engineers can use such tool to formally prove that optimized netlist produced by RTL synthesis tool is functionally equivalent to original RTL code. Additionally, designers need not have to perform gate level simulation, which is an inherently slow and time consuming task.

Figure 1: RTL-to-Gate Equivalence Checking



Approach

The various activities involved in the enhancement of the existing software to include RTL-to-gate level netlist comparison features were categorized into 3 sequential phases:

- ▶ Phase 1 essentially focused on determining the specifications and accurately estimate the effort for developing the various functionalities
- ▶ Phase 2 involved development of the bulk of the features that are relatively clear and straight forward
- ▶ Phase 3 consisted of development of the complex functionality

Members of the project team regularly interacted with the FLA team members through teleconferences and face-to-face meetings. The face-to-face meetings were held early on during the system study phase as well as towards the end of the project during the system integration stage. During the course of the project, SoftJin team members had access to the FLA systems through secure VPN access.

SoftJin developed a turnkey solution for the project that would be delivered within a fixed time frame to FLA.

Solution

In order to support RTL-to-gate capabilities, SoftJin reused the HDL front end environment. The HDL front end environment consisted of complete Verilog and VHDL parsers, Abstract Syntax Tree (AST) and Control data flow graph (CDFG) database [CDFG representation is VHDL / Verilog syntax independent]. SoftJin developed an RTL-to-gate feature based on CDFG database, which enabled RTL-to-gate capability for Verilog as well as VHDL. Please refer to Figure 1 for the architecture of the solution.

The RTL-to-gate feature used a generic library of gates to map the RTL into gates. The unoptimized netlist thus synthesized is fed into the logic equivalence checker as a reference against which the optimized and technology mapped gate level netlist [from commercially available Logic synthesis tools] was checked for equivalence.

FLA chose SoftJin to carry out the development of the RTL Inferencing tool since SoftJin has expertise in the Front End design automation area and specifically in HDL Front Ends and Synthesis tool development.

Results

The RTL-to-gate capability was demonstrated on large number of Verilog/VHDL designs, including several real life designs. The RTL designs were synthesized using commercial synthesis tool to produce optimized netlist. This netlist is then compared against original RTL code using Equivalence Checker with newly added RTL-to-Gate capability. It was observed that the Equivalence Checker correctly reported functional equivalence between original RTL design and synthesized netlist.

The engagement enabled FLA to take advantage of the off-shore EDA software development services of SoftJin. The Turnkey Project (Fixed Price) business model of SoftJin reduced FLA's risk and helped achieve its Equivalent Checker related development goals on time and with lower cost than in-house development.

Since this was a customized software development engagement, the complete rights of the developed software as well as source code were transferred to FLA. FLA is planning to re-use these components to internally develop and enhance more tools in-house in the future.

Thomas Sidle, VP, Advanced CAD Technology, FLA has this to say about the engagement – ***"SoftJin has worked with Fujitsu for a number of years on similar projects. In this project they were able to meet our goals and were honest and flexible to work all issues needed to complete the work within our constraints. We will definitely consider them for future outsourcing projects."***

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