

HIGH CAPACITY, HIGH SPEED IMAGE PROCESSING AND STORAGE SYSTEM

Customer

This case study describes SoftJin's past experience in developing and prototyping of a complex, high speed and high capacity electronic system for Japanese Industrial Equipment Company.

Project Overview

Objective:

The objective of the project is to replace a multi-processor sequential image processing system inside a industrial equipment with a FPGA and SDHC cards based large scale image storage and processing system.

Key Advantage:

The new system results in lower equipment cost and better equipment utilization due to asynchronous operation and lower power consumption.

SoftJin's Contribution:

1. To study the capacity and speed requirement of the image processing system and to come out with suitable system architecture including type of FPGA, interfaces, memory needed.
2. To develop the image storage and image transfer system on FPGA platform.
3. To develop drivers and firm-ware needed for the system.
4. To design the board schematic, layout and to develop the working prototype of the system.
5. To develop the interface between the system and PC, to develop the application running on the PC to transfer image and to control the functionality of the board
6. To identify and procure the off the shelf hardware/ software needed for the system

Top Level Architecture

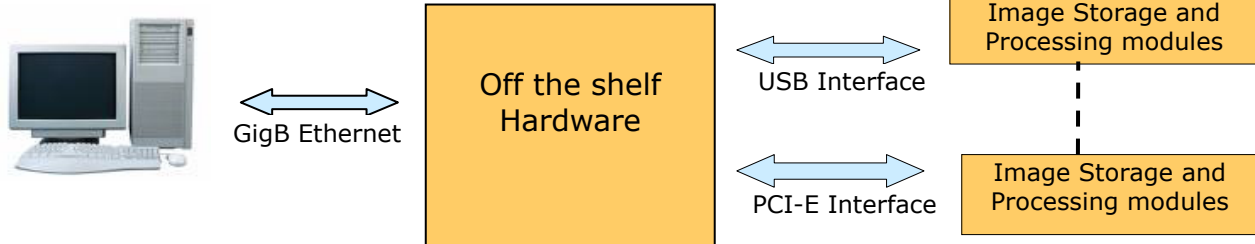
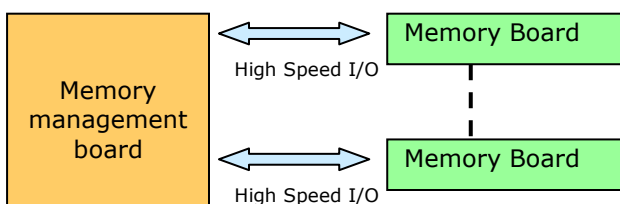


Image Storage and Processing Module Architecture



The system consists of multiple modules of image storage and processing system. Each module consists of a memory management board and a number of memory boards.

Key Challenges

1. The total system stores and processes nearly 5 TB to 10 TB of image data at a time
2. High speed data transfer (20 to 30 MB/ sec) to be achieved through the USB interface
3. High speed data transfer (80 to 100 MB/ sec) to be achieved through the PCI-E (single lane)

interface. There is a future roadmap of expanding it to eight lane PCI-E interface.

4. 40 pairs of LVDS signals (20 pairs of Tx and 20 pairs of Rx) have been used to communicate between off the shelf board and memory management board. Matched length with proper signal integrity has to be ensured in each group of 20 pairs of signals
5. Properly switching off the unused memory to reduce the power requirement of the system (to an extent of 70%)
6. Ensuring correctness of data with minimum overhead during inter FPGA communication (at a speed of 100 MHz with 32 bits data width)
7. Intelligent I/O management in FPGA with adherence to FPGA I/O banking rule due to 80% I/O utilization of the FPGA devices
8. Power distribution to multiple memory boards and handling of high current requirement
9. Intelligent memory management system to address the access of multiple memories at same time

Key Activities

Custom Board Design and Manufacturing

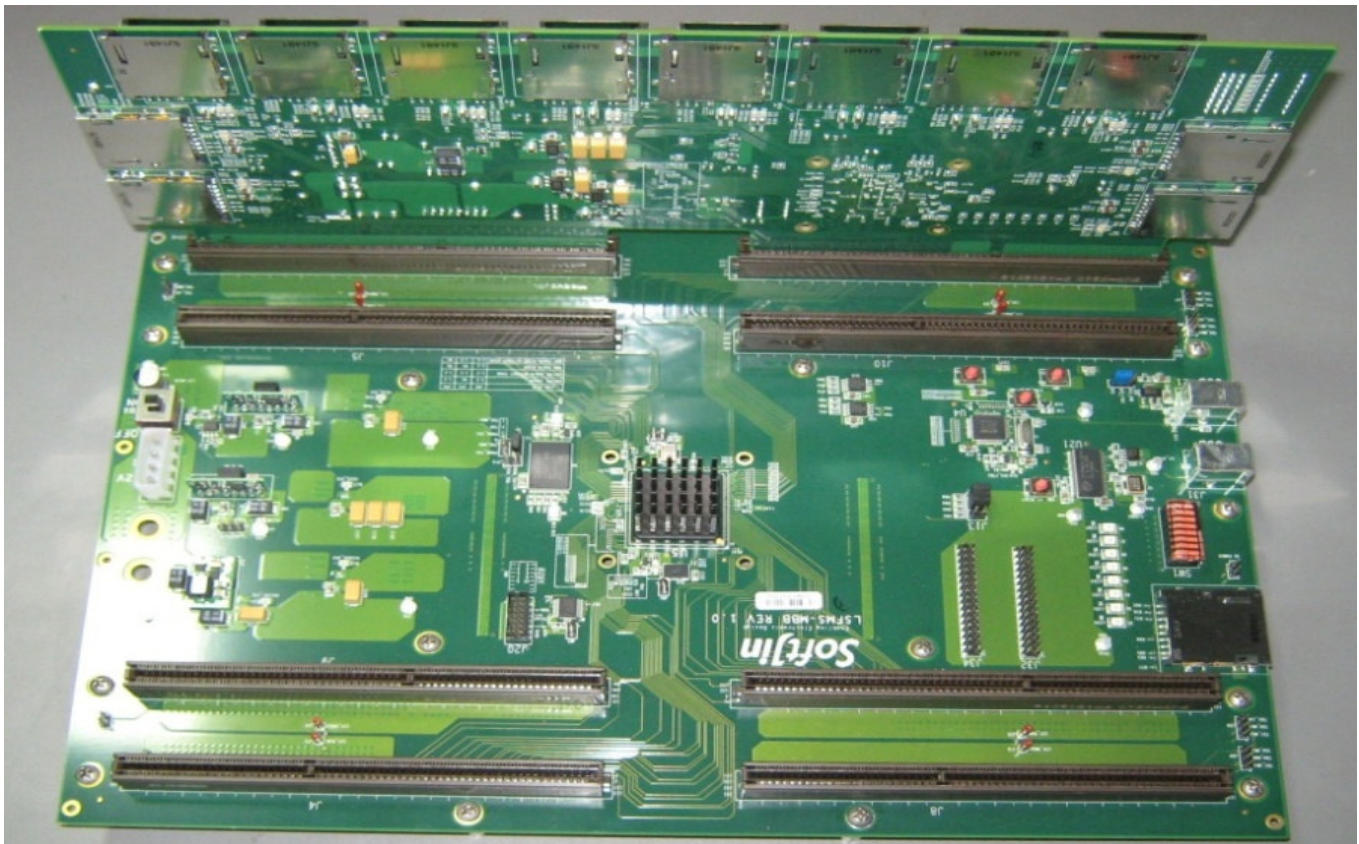
1. System architecture Design
2. Selection of key components, manufacturing process
3. Multi-board design partitioning
4. RTL development, FPGA implementation and verification of each custom board
5. Development of key FPGA modules like SD card controller, memory manager, image processing unit, USB peripheral controller
6. Schematic design, PCB layout and component placement, signal integrity test, EMI/ EMC analysis
7. Power system design, scan chain/ connector design
8. Prototype manufacturing with a PCB manufacturing partner

Integration with Off-the-shelf board and PC

1. Selection of off-the-shelf board based on System requirements
2. Design of communication protocol between off-the-shelf hardware and custom board
3. Integration of the Custom board and off-the-shelf board

Software Development and Integration

1. Firmware, driver development
2. Application software development including Operator Control and monitoring GUI
3. Porting of the software on the prototype system and full system testing



Picture shows one Image Processing and Storage Module consisting of a Memory Base Board and one Memory Board (having multiple SDHC cards)