

Data sheet for Audio Processor Core

Functional Description

This document describes the verilog model for 24-bit audio processor, which support move, arithmetic and loop instructions. The processor can be programmed using assembly language.

Features:

- 24 bit addressing
- 7 stage pipeline architecture
- Single clock cycle per instruction
- Configurable program/data memory (default size of X/Y RAM is 4k x 24 and of Prog RAM is 16k x 24)

Block Diagram:

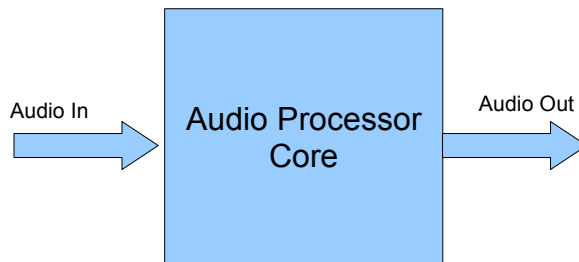


Figure 1: Block diagram

Architectural Diagram:

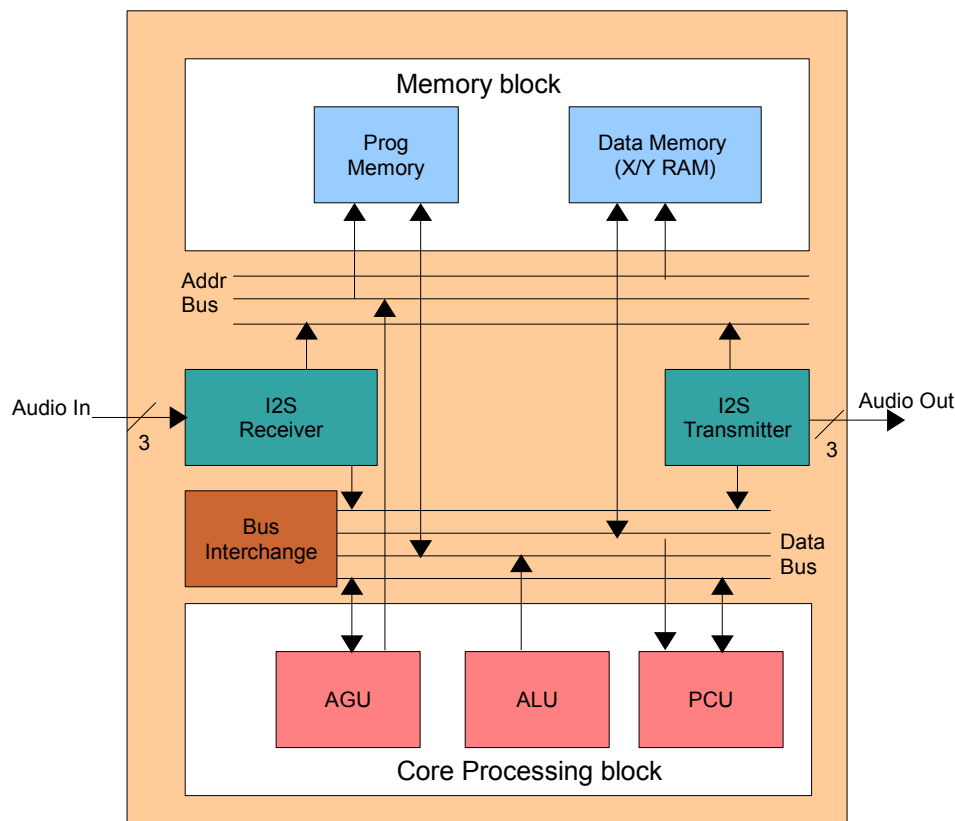


Figure 2: Audio processor architecture

Description:

1. Core processing block contains
 - Program Control Unit (PCU)
 - Arithmetic Logic Unit (ALU)
 - Address Generation Unit (AGU)
2. 16K x 24 program memory and 4K x 24 data memories (X and Y).
3. 24 bit data and address buses to read/write data into X, Y, P memories and peripheral

interface.

4. Supported instructions are MOVE, ADD, MPY, MAC, ASR, ASL, ADDL, ADDR and DO
5. Supports different addressing modes (Immediate, absolute, register direct, register indirect, post increment/decrement by offset or constant etc.)

Program Control Unit (PCU) model:

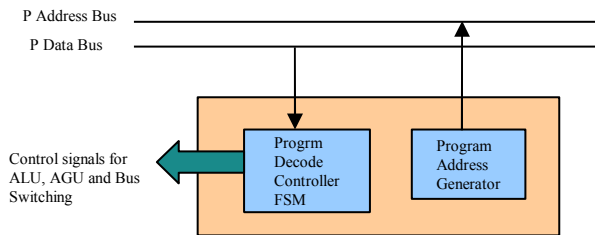


Figure 3: Program Control Unit

1. PCU coordinates execution of instruction and generates control signals for ALU, AGU and bus switching
2. PCU is composed of
 - Program Decode Controller
 - Program Address Generator
3. Program decode controller decodes 24-bit instructions and generates signals for
 - Pipeline control,
 - data move operation between memory and registers
 - arithmetic operations

PCU Program Address Generation Unit:

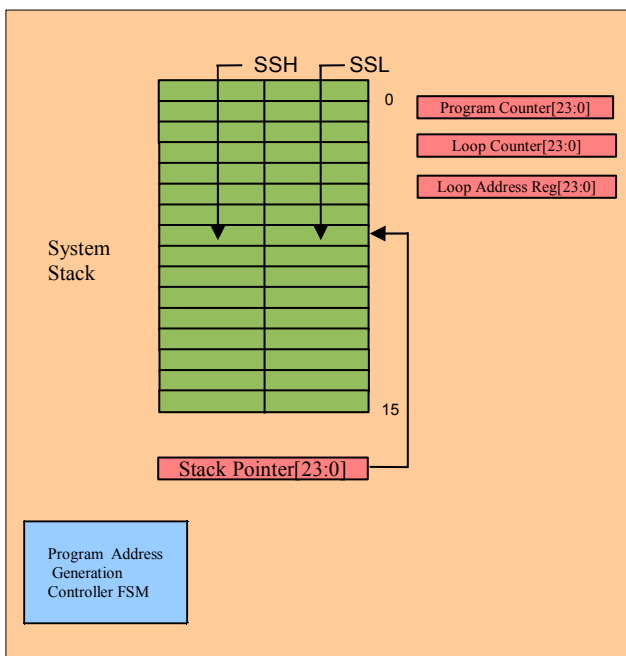


Figure 4: PAG model

1. PAG contains a controller FSM and hardware for program address generation
2. The hardware includes
 - 24 bit program counter, loop counter, loop address register, stack pointer
 - system stack of 16 x 48
3. The PAG controller FSM generates necessary control signals to control the programmable registers.

Arithmetic Logic Unit:

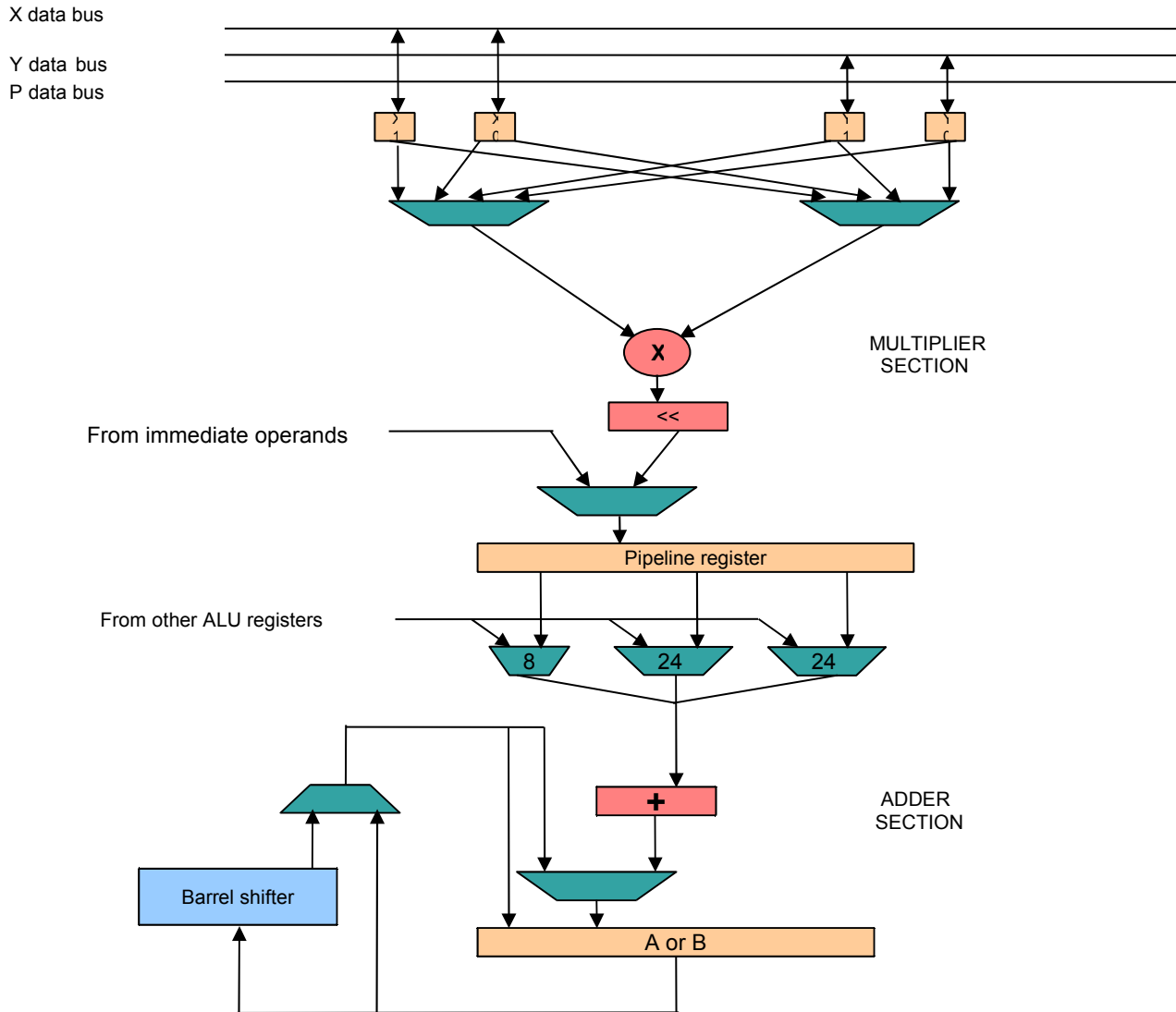


Figure 5: ALU model

ALU Description:

- 24 bit data input registers X0,X1,Y0,Y1 which can be operated as either 4 independent 24 bit registers or two 48 bit registers X, Y
- Data accumulator registers: A2,A1,A0; B2,B1,B0
 - (A2,A1,A0) and (B2,B1,B0) form two 56-bit accumulator registers
 - A is A2:A1:A0 and B is B2:B1:B0
 - A2 & B2 are 8-bit "extensions," rest are 24-bit
- MAC and Logic Unit
 - performs all calculations: \times , $+$, $-$, shift
 - up to 3 input operands,
 - result must be in A-Accumulator or B-Accumulator

Address Generation Unit:

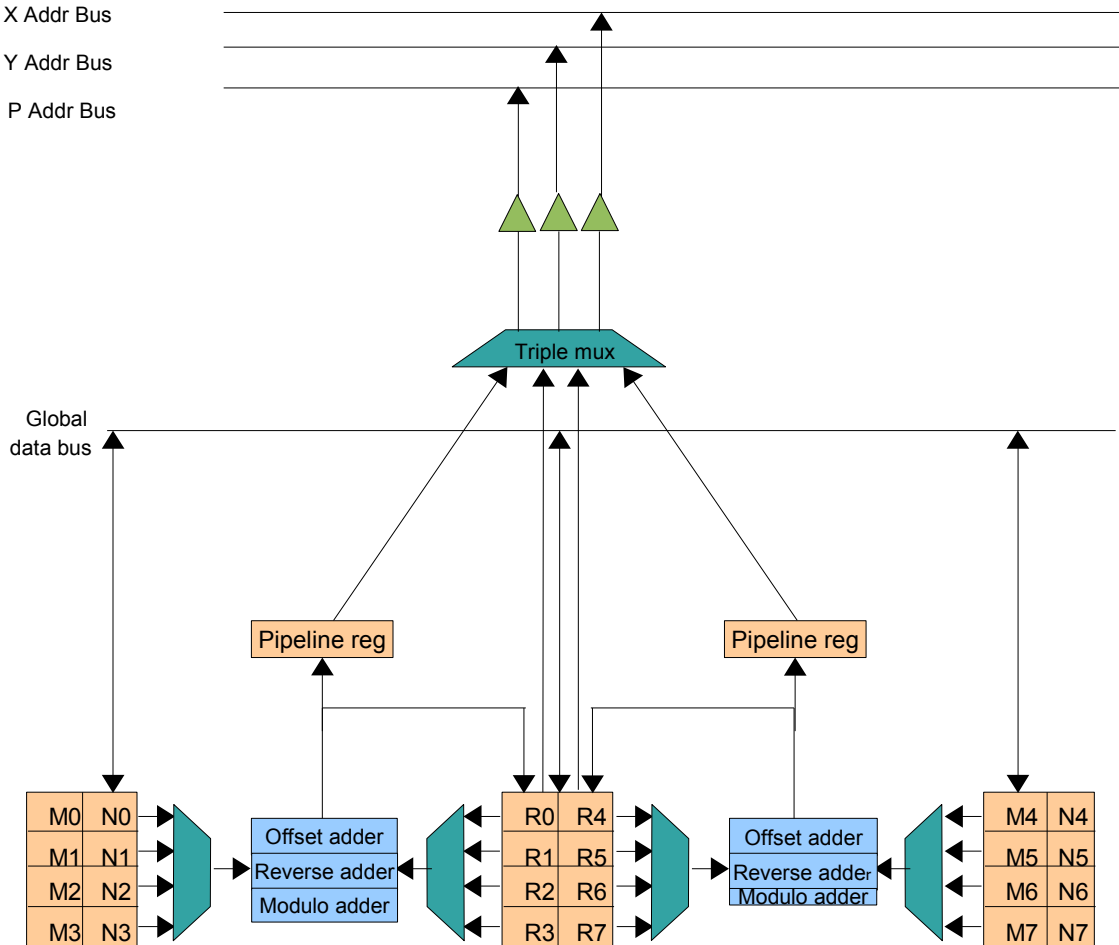


Figure 6: AGU architecture

AGU contains

1. 8 16-bit Address Registers R0. . . R7 that point to memory locations
2. 8 16-bit Offset Registers N0. . . N7 that are added to the respective Rn to form the final address
3. 8 16-bit Modifier Registers M0. . .M7 that specify type of arithmetic to update Address Register
4. 3 types adders : offset adder, modulo adder and reverse adder
5. Triple mux to select address lines

Signal definition table:

Signal	Direction	Description
clock	IN	This is the system clock.
reset	IN	This is the system reset.
I2S In	IN	This is 3 bit (system clock (SCK), serial data (SD) and word select (WS))
I2S Out	Out	This is 3 bit (system clock (SCK), serial data (SD) and word select (WS))

Schematic Symbol

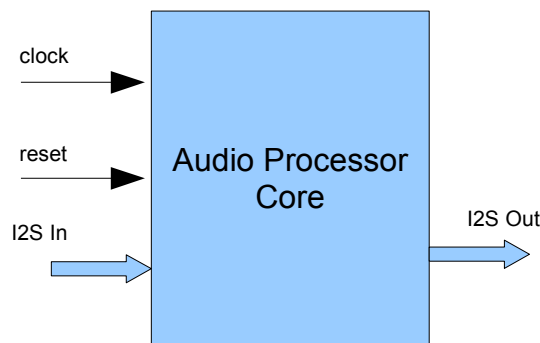


Figure 7: Schematic Symbol

Performance:

Device	Slice LUTs	Slice Flops	Frequency
Virtex-5	5687	5927	98 MHz

Verification:

The Audio processor module has been verified with following approaches:

- Exhaustive Functional/Timing simulation.

Deliverables:

- Verilog RTL source code
- Test benches
- Synthesis and Simulation scripts.
- Detailed user documentation, including RTL source code documentation