

Video Frame Buffer

Functional Description

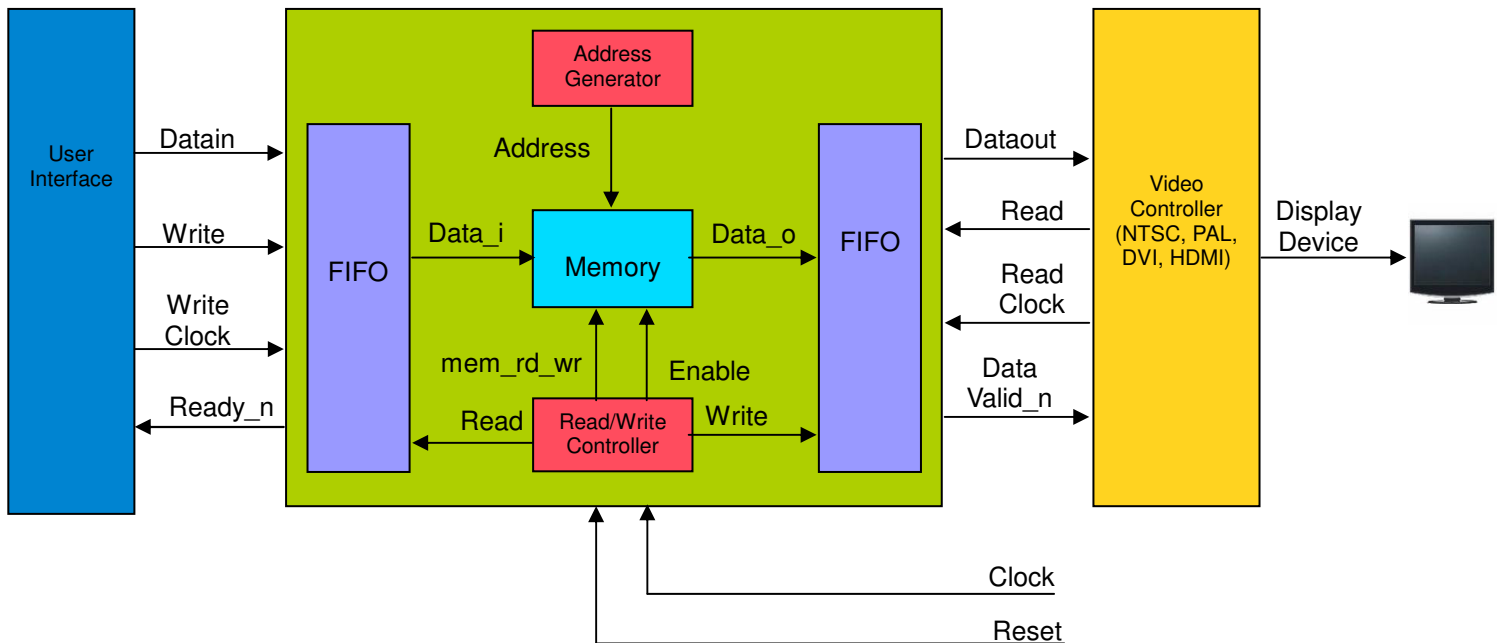
Video frame Buffer holds the video data to be displayed on output devices such as TV, projectors. Video buffer stores the data into memory in different width format as required by the application. It enables synchronization of data across different clock domain as well as different format domain. The read and write request will be sent from external interface, internally controller resolves the request and updates the contents of video buffer.

It supports continuous data stream to/from external interface with the help of entry and exit FIFOs.

Features

- Configurable Frame size
- Data frame rate conversion
- Constant Input/output pixel data rate
- Memory model can be replaced with BRAM, SRAM, DDR memory or any external memory depending on application.

Block Diagram



Performance:

Device	Slice Count	LUT Count	Frequency (MHz)
Spartan-3A (xc3s700A)	207	261	100+

Verification:

The Video Buffer core has been verified with following approaches:

- Exhaustive Functional/Timing simulation.
- Tested with Video frames for DVI transmitter and NTSC/PAL video.

Deliverables:

- Verilog RTL source code
- Test benches
- Synthesis and Simulation scripts.
- Detailed user documentation, including

RTL source code documentation

Applications

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- DVI/HDTV/NTSC-PAL video interface
- Digital Photo frame
- Set-Top boxes
- Frame Synchronization

Typical Application:

