

Universal TV Encoder

Introduction

SoftJin's Universal TV Encoder IP accepts BT 601/656 or BT 709/1120 video stream as input and generates a high quality SD / HD video stream accepted by a wide range of SD and HD Display devices. It supports most of the popular video standards supported by SD/HD TV.

This makes the Universal TV Encoder IP as an ideal building block for SoC or FPGA based Systems targeting Set-top-box, Media players, DVD players and digital camera processors etc.

The key blocks which make this encoder "universal" are

- Motion adaptive de-interlacer
- SD to HD Upscaler
- NTSC/PAL/SECAM Encoder

- High Definition Analog Encoder(YPbPr)
- HDMI Tx

Features

Input Formats Supported:

- BT601, BT656 and BT 709/1120
- Interlaced and non interlaced

Output Formats Supported:

- SD Video: NTSC, PAL, SECAM 480i/576i
- HD Video: Analog (YPbPr) and Digital (HDMI)
- HD Video: 480p/576p/720p/1080i/1080p
- Composite, S-video, Component video
- Internal Color Bar mode

Format Conversion:

- De-interlacing and up-scaling of SD to HD

Functional Description

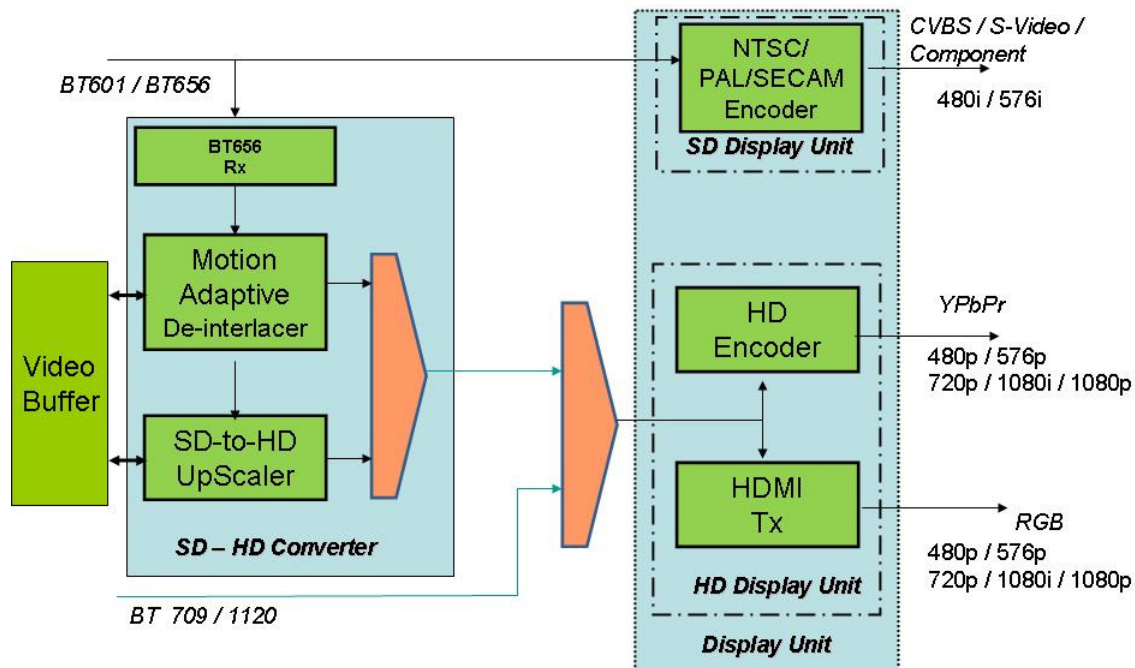


Figure 1: Block Diagram Universal TV Encoder

Universal TV Encoder consists of 3 main blocks:

- **SD-HD Converter:** This block consists of two components: Motion Adaptive De-interlacer and SD-to-HD upscaler. Motion Adaptive De-interlacer module uses adaptive de-interlacing algorithm to convert interlaced video to progressive video format. SD-to-HD upscaler module reads the progressive video frame and upscales to high definition resolution 720p or 1080p using proprietary scaling algorithm. Motion Adaptive de-interlacer and SD-to-HD upscaler components use external 8MB DDR memory as video frame buffer.
- **SD Display Unit:** This block consists of NTSC/PAL/SECAM Encoder which supports video encoding in NTSC, PAL and SECAM video standards. It supports simultaneous CVBS, S-video and Component video outputs. An external 10 bit DAC is required along with the NTSC/PAL/SECAM encoder for converting digitally encoded video to analog format.
- **HD Display Unit:** This block consists of two sub-blocks for analog and Digital HDTV video encoding standards.
 - For Analog HDTV, the HD Encoder block generates 10-bit YPbPr components outputs. It supports 480p/576p/720p/1080i/1080p resolutions. HD Encoder needs an external 10bit DAC to convert digitally encoded video to analog format.
 - For Digital HTDV, the HDMI Tx block encodes video data using TMDS 8bit-to-10bit encoding and sends out the HD output serially using differential signaling. It supports 480p/576p/720p/1080i/1080p resolutions.

I/O Ports:

I/O ports for Universal TV Encoder are summarized in Table1.

Table1 I/O Ports

Port Name	Direction	Width (bit)	Description
BT 601	Input	8	Standard BT601/BT656 video stream
BT 709	Input	8/16	Standard BT 709/BT1120 video stream
SD Output (for external DAC(s))	Output	60	All SD video formats are simultaneously available at output.
SD_CVBS	Output	10	For single DAC interface
SD_S-Video	Output	20	For 2 DACs interface (Y,C)
SD_Component	Output	30	For 3 DACs interface (RGB, YUV)
Analog HD Output	Output	30	For 3 DACs interface (YPbPr)
HDMI Tx	Output	4 TMDS differential pairs	3 pairs for RGB data, 1 pair for pixel clock

Test Setup:

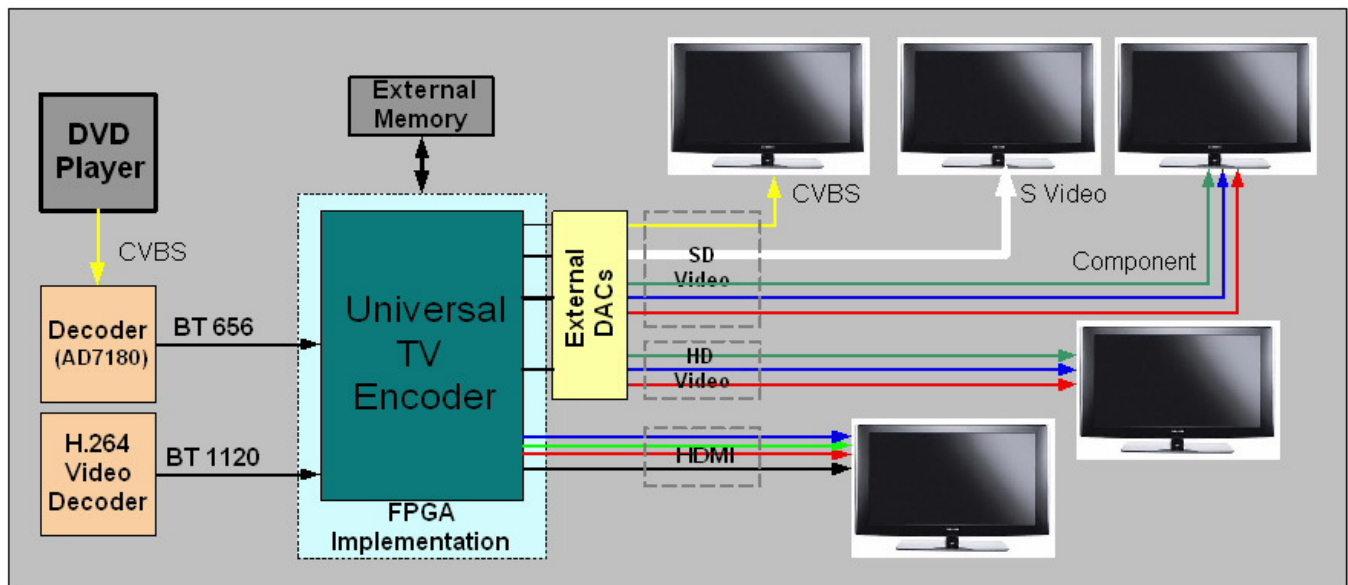


Figure 2 Test Setup

Universal TV Encoder IP is thoroughly tested along with various SD/HD televisions. A typical usage of Universal TV Encoder in a test setup shown in. Figure 2.

Universal TV Encoder IP functionality has been proven on Altera and Xilinx FPGA

Input signals generation scheme:

- An off-the shelf DVD Player used to generate CVBS format video stream.
- Video Decoder AD7180 from Analog Devices, used to generate BT656 stream.

Output signals generation scheme:

- For SD and HD video signals external DACs are used. Total 9 DACs would be needed if all analog video signals are to be viewed simultaneously on 4 separate TVs
- HDMI signals are connected from FPGA to TV with just ESD protection circuit in between.

Deliverables:

- Verilog RTL source code
- Detailed documentation