

USB - FPGA Host/Peripheral Interface IP

Functional Description:

The USB-FPGA interface IP is an easy to use interface between USB 2.0 compliant host/peripheral devices and FPGA.

Features:

- Supports USB Host and Peripheral interface
- Supports USB 2.0 interface to FTDI FT2232H and Cypress FX2 modules
- Supports USB 1.1 interface to FTDI FT2232L
- Tested on Spartan3A and Virtex4 devices

USB Host Interface:

This enables interface with USB devices such as Flash drive. Using this IP, the files stored in flash drive can be read or written through simple SPI or FIFO interface.

This IP provides an interface with USB FTDI VNC1L Host Controllers. The VNC1L is a "single chip" embedded USB host controller. Amongst many good features of this host controller, two key features are:

- Integrated firmware allows read/write access to FAT32 formatted USB Flash drive
- Entire USB protocol handled on the chip

The on-chip firmware supports simple command set to read/write file from USB flash drive.

As shown in Figure 1, this interface is very useful in FPGA based stand-alone systems, where USB flash drives are to be used as storage devices.

The USB host interface IP handles the communication protocol to interact with USB host device, using serial SPI protocol.

A compact FPGA stand-alone system can be developed and applications such as data-loggers,

pattern generators can be developed around it.

USB Peripheral Interface:

This IP enables high-speed two-way communication between FPGA and PC. The IP is targeted for interfacing FPGA with industry popular USB peripheral chips such as FTDI's FT2232L, FT2232H and Cypress FX2 devices.

The FTDI FT2232H and Cypress FX2 are USB 2.0 compliant devices. With the help of these devices, data transfer rates as high as 20M Bytes per second are achieved between PC and FPGA.

FT2232L is USB 1.1 compliant device; hence transfer rates up to 1.5M Bytes per second can be achieved.

These devices have connectivity to PC via USB cable and at the other end parallel bus connection is made available to interface with FPGA.

Thus, these USB peripheral devices:

- Terminate USB protocol transactions and present raw data at the output of device to FPGA
- Accept raw data from FPGA and add USB protocol overheads and sends data back to PC.

As shown in Figure 2, IP consists of a Peripheral Controller which talks to USB peripheral device as per peripheral device specific protocol. It arbitrates between the Transmit and Receive data path as per data availability in Tx or Rx FIFO.

It stores data received from PC side into Rx FIFO and picks-up data to be sent to PC from Tx FIFO

Block Diagram:

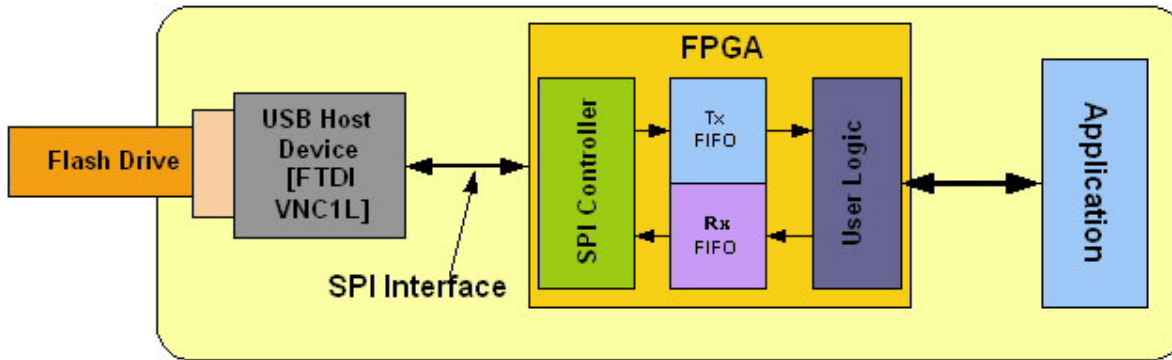


Figure 1. USB Host Controller Interface

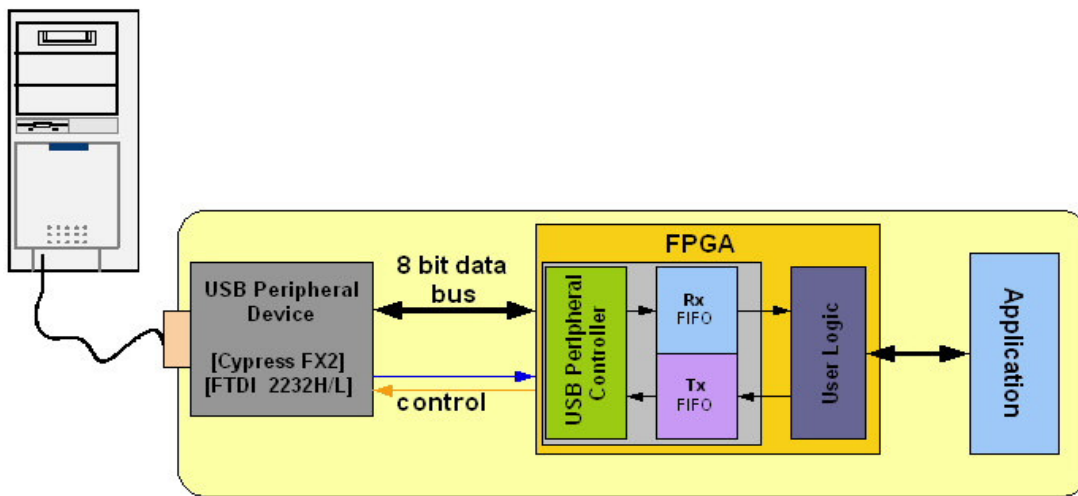


Figure 2. USB Peripheral Controller Interface

Performance:

S. No	USB Interface Type	Name of the Controller	DFF	LUT4	I/Os	RAMB16s	Transfer Speed MB/s	Clock between FPGA and USB device MHz
1	Peripheral	FTDI 2232L USB 1.1 parallel interface	17	41	12	--	1.5	12.5
2		FTDI 2232H USB 2.0 parallel interface	442	353	14	2	20	60.0
3		Cypress FX2 USB 2.0 parallel interface	664	547	21	4	14	48.0
4	Host	FTDI VNC1L USB 2.0 serial interface	47	65	4	--	0.4	12.5

Verification:

The Video Encoder module has been verified with following approaches:

- Simulations using Xilinx ISE and Mentor's Modelsim.
- Prototyped on Spartan3A and Xilinx ML401 Board

Deliverables:

- Verilog RTL source code
- Test benches
- Other Behavioral models required for simulation