

Semi Parallel FIR Filter

Functional Description

This version of Semi Parallel Finite Impulse Response Filter uses 4 Multipliers and 5 Accumulators. Each MAC unit has a dedicated Co-efficient ROM and Data Shift Register. For a 16 tap filter each MAC unit computes 4 partial products. The 5th accumulator computes the final product by adding the results of all the MAC units.

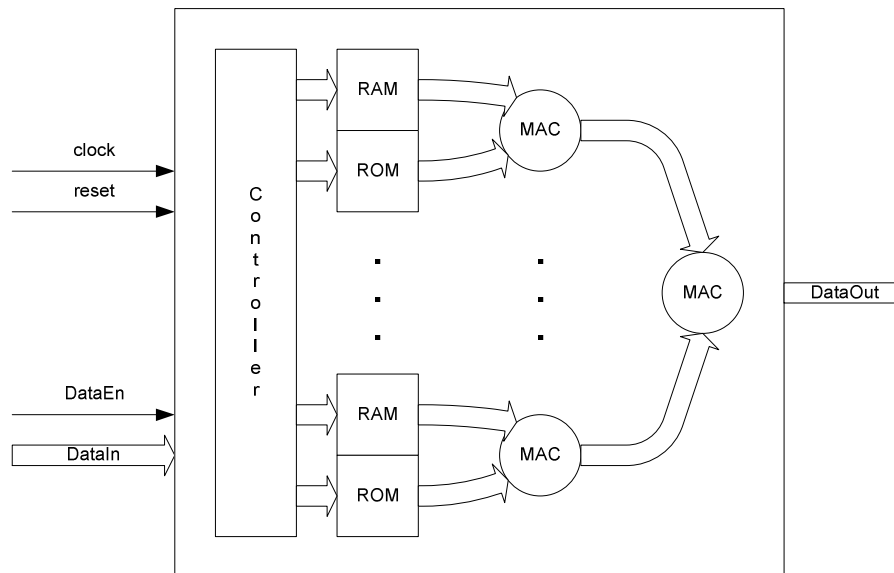
This version can be easily extended to 97 tap filter

by increasing the depth of Co-efficient ROM & Shift register and making appropriate changes to the Controller module.

Features:

- Number of taps can be configured.
- Input data width and coefficient width can be configured.
- Area efficient implementation.

Block Diagram:



Performance:

Device	Slice Count	MULT18x18	Frequency
Spartan-3A (xc3s700a-4fg484)	198	4	176 MHz
Virtex-4 (xc4vlx25-12ff668)	262	0	236 MHz

Verification:

The Semi Parallel FIR Filter module has been verified with exhaustive Functional and Timing simulation

Deliverables:

- Verilog RTL source code
- Test benches
- Synthesis and Simulation scripts
- Detailed user documentation, including RTL source code documentation