

Datasheet for ZBT SRAM Controller

Functional Description

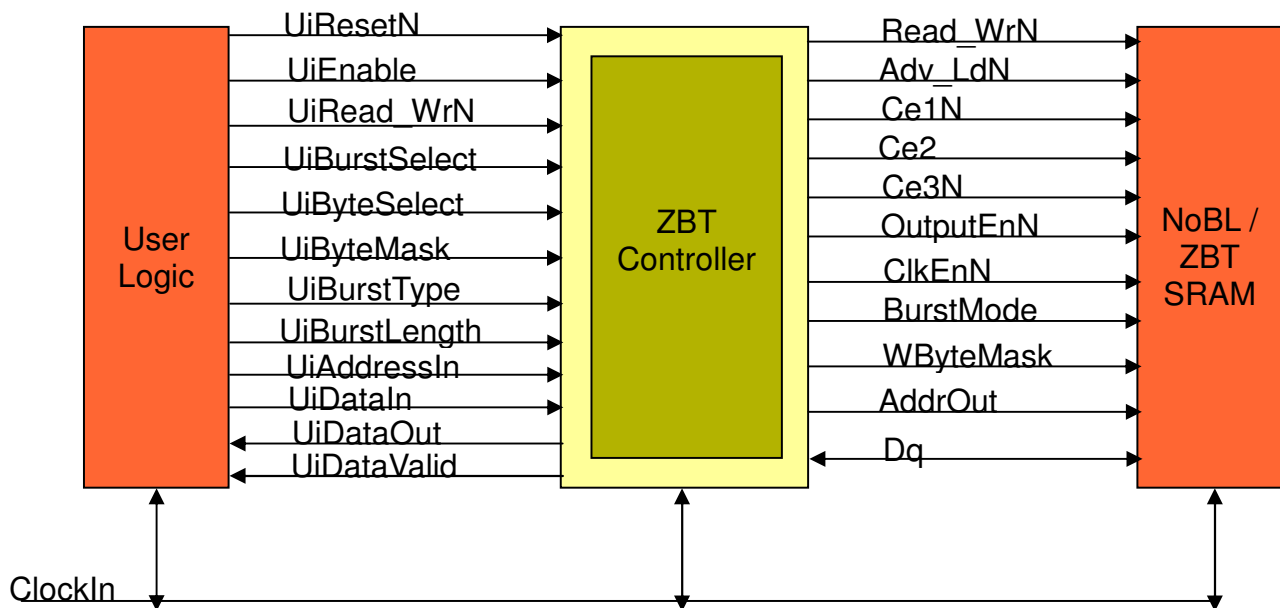
The ZBT SRAM Controller core is a versatile, scalable module interfaces with Cypress CY7C1354B synchronous pipelined burst SRAM with NoBL(No Bus Latency) logic, which is functionally equivalent to synchronous pipelined ZBT (Zero Bus Turnaround) SRAM families from Micron and IDT.

The ZBT SRAM controller accepts SRAM request from user and performs pipelined read and write operations. The controller ensures that correct latencies and bus turnaround timings are met.

Features:

- Supports 256K X 32 ZBT SRAMS and scalable.
- 18 to 24 address lines and 32 bit data bus
- Single word read and write cycle
- Burst mode with 2/4 word cycles
- linear or interleaving burst mode selection
- Selective Byte write

Block Diagram:



Signal Description:

Signal Name	Signal Width	Direction (I/O)	Description
ClockIn	1	I	Clock signal drives ZBT controller logic and ZBT SRAM memory .
UiResetN	1	I	ZBT controller reset signal . Active low.
UiEnable	1	I	ZBT controller enable signal .

UiRead_WrN	1	I	Read / write control signal to ZBT controller; High selects read operation. Low selects write operation.
UiBurstSelect	1	I	Burst/Single R/W operation selection signal . High select burst R/W operation. Low selects Single R/W operation.
UiBurstType	1	I	Burst order selection signal. High selects interleaved burst order. Low selects linear burst order.
UiBurstLength	1	I	R/W Burst length selection signal. High selects burst cycle of 4. Low selects burst cycle of 2.
UiByteSelect	1	I	Write Byte Mask Enable Signal. High enables Write Byte Mask option. Low disables write Byte Mask option.
UiByteMask	[3:0]	I	Masks the Bytes in write mode. Logic 1 in the mask field indicates write is allowed for that byte. LSB corresponds to Byte1.
UiAddressIn	[17:0]	I	ZBT controller address bus (scalable)
UiDataIn	[31:0]	I	ZBT controller input data bus (scalable)
UiDataOut	[31:0]	O	ZBT controller output data bus (scalable)
UiDataValid	1	O	Data Valid Signal to user.
Read_WrN	1	O	R/W control signal to ZBT SRAM
Adv_LdN	1	O	Advance or Load(active low) control signal to ZBT SRAM
Ce1N	1	O	Chip enable 1 (active low) signal to ZBT SRAM
Ce2	1	O	Chip enable 2 (active high) signal to ZBT SRAM
Ce3N	1	O	Chip enable 3 (active low) signal to ZBT SRAM
OutputEnN	1	O	Output Enable (active low) signal to ZBT SRAM
ClkEnN	1	O	Clock Enable (active low) signal to ZBT SRAM
BurstMode	1	O	Burst mode selection signal to ZBT SRAM
WbyteMask	[3:0]	O	Write Byte Mask (active low) signal to ZBT SRAM
AddrOut	[17:0]	O	Address signals to ZBT SRAM (scalable)
Dq	[35:0]	I/O	Bi-directional Data I/O lines

Performance:

Device	Slice Count	Frequency
Xilinx Virtex4	65	100 MHz

Verification:

The ZBT SRAM controller module has been verified with following approaches:

- Exhaustive Functional/Timing simulation
- Prototyped on Xilinx Virtex ML401 development board

Deliverables:

- Verilog RTL source code
- Test benches
- Synthesis and Simulation scripts
- Detailed user documentation, including RTL source code documentation