

SPI Master Controller

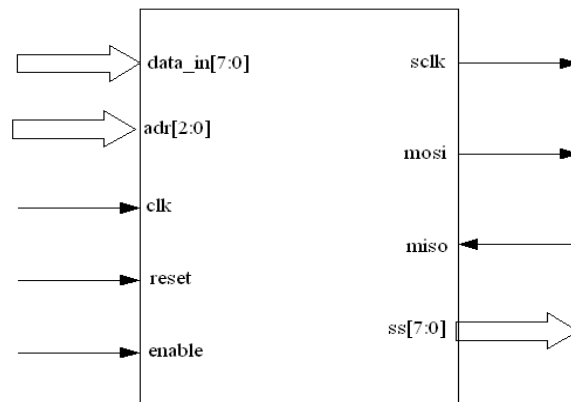
Functional Description:

The Serial Peripheral Interface (SPI) is a serial, synchronous communication protocol that is standard across microprocessors, microcontrollers and peripherals. It provides interfaces between different devices such as microcontrollers, microprocessors, ADC's, DAC's, flash memories and other. SPI Master Controller Core implements master functionality of the SPI protocol. The controller can be configured to support various features listed below.

Features:

- Full duplex serial data transfer
- MSB or LSB data transfer first
- Receiving and transmitting on both receiving and falling edges of the clock independently
- 8 slave select lines
- Supports multi slave operation
- Standard Verilog Soft core
- Fully Synthesizable

Symbol:

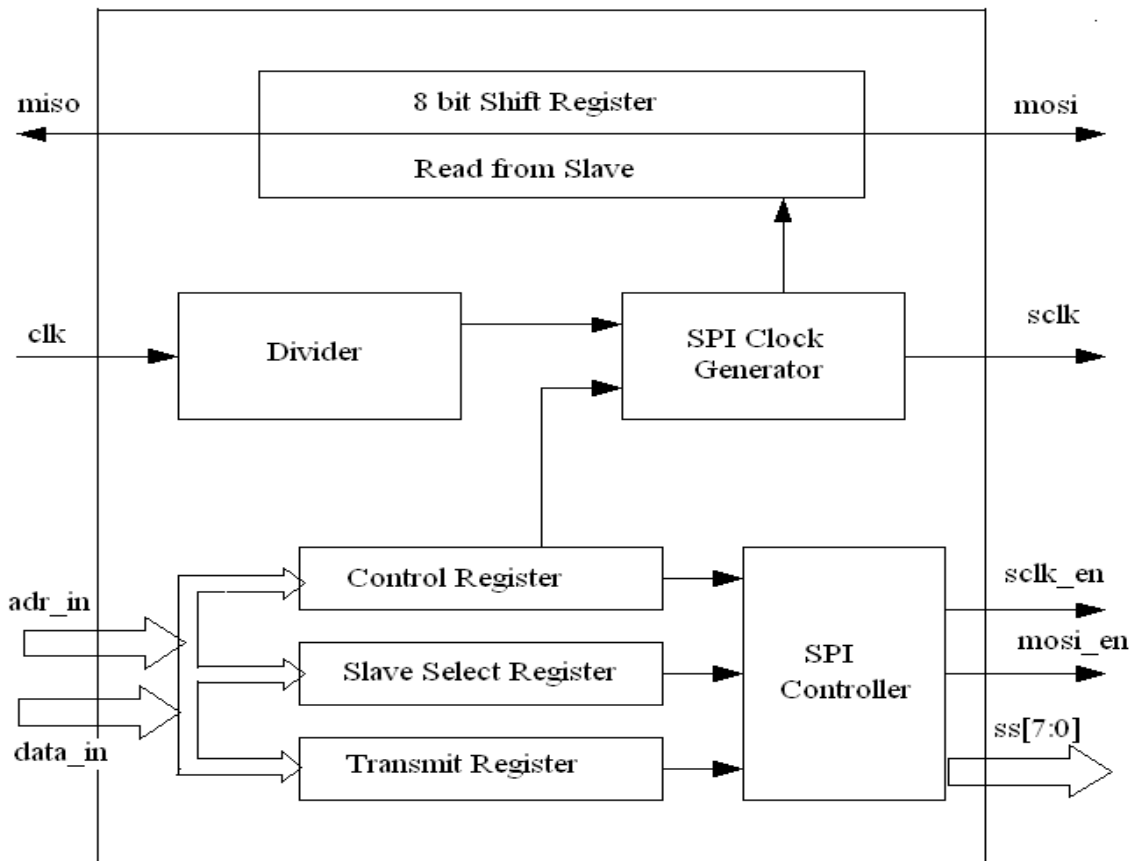


Pin Descriptions:

Pin	Type	Description
data_in[7:0]	input	Data bus input
adr[2:0]	input	Address line
Clk	input	Master clock input
Reset	input	Reset pin
Enable	Input	Enable Pin
Sclk	output	SPI clock output
Mosi	output	Master out-Slave in line

Pin	Type	Description
Miso	Input	Master in-Slave out line
ss[7:0]	output	Slave Select line

Block Diagram:



Functionality of the sub-blocks is given below:

- **8 bit Shift Register and Read from slave:** It is the Central element in the SPI system. While an SPI transfer occurs, 8 bit data is shifted out of the SPI line, simultaneously the 8 bit data coming from the slave is shifted in or stored in the register. As a result during one cycle of transmission the master and slave will have effectively exchanged their data.
- **Control Register:** This register may be read or written at any time. It controls the

data transfer. This register is used to controls different configuration like start of transmission, LSB or MSB first, transmission and reception under negative or positive edge etc.

- **Slave Select Register:** Configures which slave select output should be driven on SPI master transfer. The contents of this register drives the particular output pin on **ss[7:0]** line.
- **Transmit Register:** This register is used to hold the data that is to be transmitted.

- **Divider and SPI Clock Generator:** The contents of the divider register specify the frequency of the SPI clock(sclk) based on the input clock(clk) given by the equation

$$f_{sclk} = f_{clk} / (\text{divider} + 1) * 2$$

- **SPI Controller:** This block is used to control the overall operation of the SPI master system.

Performance:

Device	Slice Count	Frequency
Spartan-3A (3s700anfg484-4)	41	179 MHz
Virtex-4 (4vsx25ff668-12)	44	385 MHz

Deliverables:

- Verilog RTL source code
- Test benches

- Synthesis and Simulation scripts
- Detailed user documentation, including RTL source code documentation