

Data sheet for S/PDIF transmitter

Functional Description

This document describes S/PDIF (Sony/Philips Digital Interconnect Format) digital audio transmitter. The core supports up to 24 bits per sample and up to 192 kHz sample rate. It supports linear PCM and non linear PCM audio streams in both consumer and professional applications.

Features:

- Conforms to IEC-60958, AES/EBU, AES3 standards
- Variable sample rate support including (32-192 kHz)
- Audio data FIFO with configurable size and audio sample length (16/20/24)
- Compact, high-performance architecture

Block Diagram:

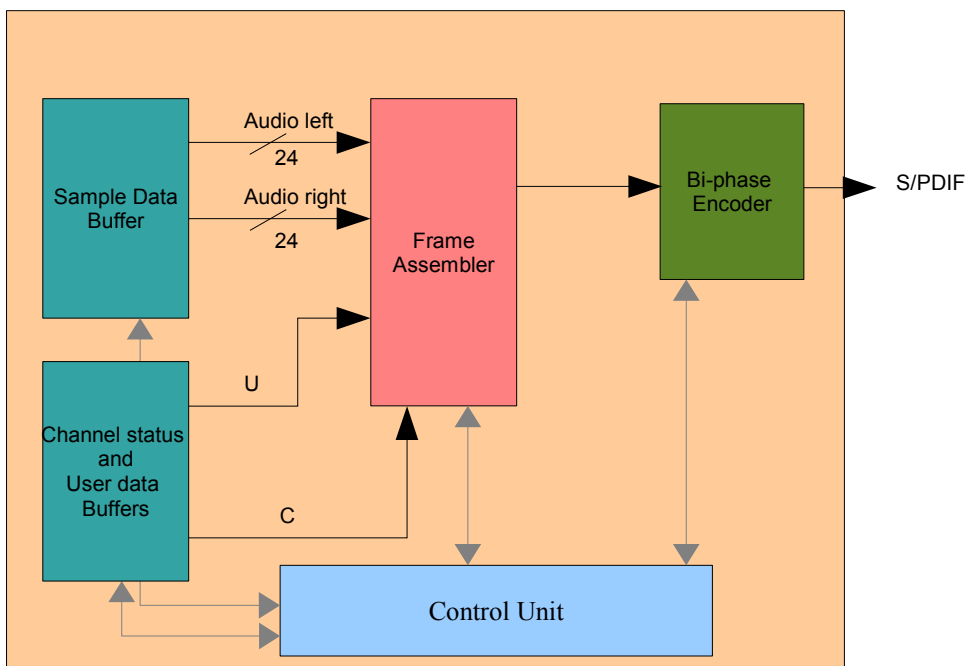


Figure 1: S/PDIF transmitter architecture

Description:

Audio data are stored in Sample Data Buffer. The size of buffer is configurable, default is 1024 words (512 words for both left and right channel). Audio sample length is also configurable (16/20/24 bit). The Channel Status and User Data streams are

stored in two different buffers. The core can generate channel status word or use external channel status word from the buffer. Frame assembler generates parity bit, crc (if channel status word to be generated) and assembles the frame.

Signal definition table:

<i>Signal</i>	<i>Direction</i>	<i>Description</i>
clock	IN	This is the system clock.
reset	IN	This is the system reset.
S/PDIF Out	Out	1 bit bi-phase encoded spdif signal

Performance:

Device	Slice LUTS	Slice Flops	BRAM
Virtex-5	133	204	2

Verification:

The S/PDIF transmitter module has been verified with following approaches:

- Exhaustive Functional/Timing simulation.

Deliverables:

- Verilog RTL source code
- Test benches
- Synthesis and Simulation scripts.
- Detailed user documentation, including RTL source code documentation