

## Datasheet for SD Controller

### Functional Description

The SD controller provides easy to use interface for the user to communicate with SD card. The controller has a very flexible and programmable interface which will support both SD and SD4 modes.

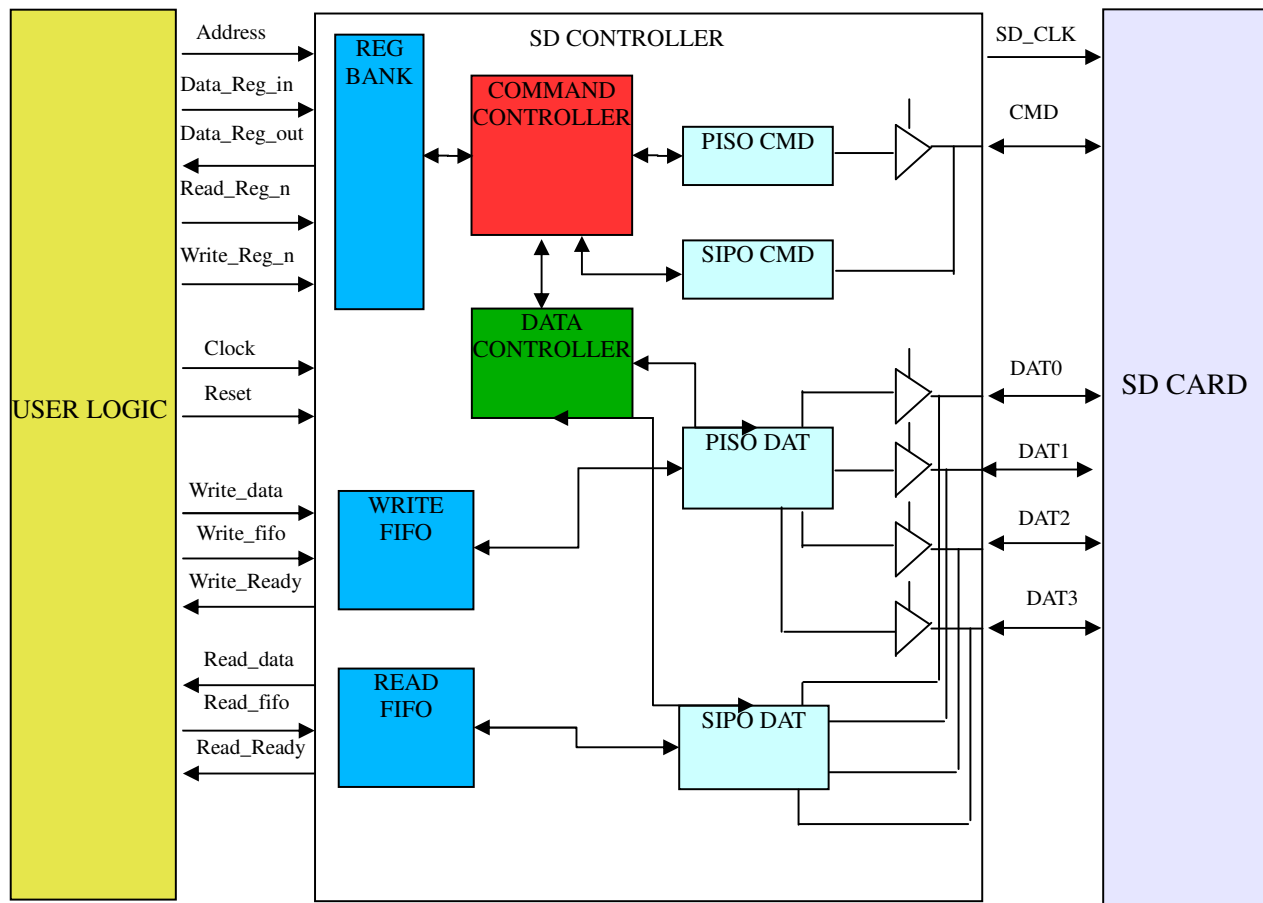
### Features

- Meets SD physical layer specification version 2.00.
- Supports standard SD memory cards and High

capacity SD memory cards.

- Supports both SD and SD4 operation modes.
- Supports multiple block read and multiple block write operations.
- Inbuilt CRC7 and CRC16 generators to check the data integrity.
- Supports variable block lengths (8,512,1024...etc)
- Flexible architecture and simple user interface to carry out SD card operations.

### Block Diagram:



### Description:

<i>Block</i>	<i>Description</i>
Register Bank	The controller's functionality is configured and controlled by setting specific registers.
Write FIFO	Contains block of data which is to be written into the SD card is stored in this FIFO before write command is issued.
Read FIFO	After a successful read operation from SD card , Data obtained from SD card is stored here.
CMD Controller	Command Controller is the Master device which controls all the other peripherals. It also controls sending commands and receiving response from SD card.
DAT Controller	Data controller controls the transfer of data from controller to SD card and vice versa.
PISO CMD	Transfers command over the CMD line and append CRC7 code.
SIPO CMD	Receives serial response from SD card and verifies CRC7.
PISO DAT	Transfer data with CRC16 over DAT0-DAT3 lines.
SIPO DAT	Receives data and analyzes CRC16 from DAT0-DAT3 lines.

### Pin Description:

<i>I/O Name</i>	<i>Width</i>	<i>I/O direction</i>	<i>Description</i>
Clock	1	Input	Board clock input to the controller module.
Reset	1	Input	Asynchronous active high reset for controller module.
Address	5	Input	Address input to access the register bank.
Data_reg_in	16	Input	Data input to the register bank.
Data_reg_out	16	Output	Data output from the register bank.
Read_reg_n	1	Input	Active low read enable for register bank.
Write_reg_n	1	Input	Active low write enable for register bank.
Write_data	8	Input	Data input to the FIFO.
Read_data	8	Output	Data output from FIFO.
Write_fifo	1	Input	Write enable for FIFO.
Read_fifo	1	Input	Read enable for FIFO.
Write_ready	1	Output	On active high, FIFO is ready to receive data.
Read_ready	1	Output	On active high FIFO is ready to send data.

<i>I/O Name</i>	<i>Width</i>	<i>I/O direction</i>	<i>Description</i>
SD_CLK	1	Output	Clock output to SD card.
CMD	1	Bidirectional	CMD line of SD card.
DAT0	1	Bidirectional	DAT0 line of SD card.
DAT1	1	Bidirectional	DAT1 line of SD card.
DAT2	1	Bidirectional	DAT2 line of SD card.
DAT3	1	Bidirectional	DAT3 line of SD card.

**Performance:**

<i>Device</i>	<i>Slice count</i>	<i>LUT count</i>	<i>Maximum Frequency</i>
Spartan3a - 3s700afg484	1983	2760	146.456Mhz
Virtex4-xc4vlx25ff668	2066	2904	205.090Mhz

**Verification:**

The SD controller module has been verified with following approaches:

- Exhaustive Functional/Timing simulation using a SD card behavioral model.
- Prototyped on Xilinx Spartan-3A and Virtex-4 development boards.

**Typical Applications:**

- SD Audio Application: The SD controller was interface with Xilinx Microblaze processor and
- source code documentation

with an AC97 controller an audio application was developed.

- FAT32 Application: Developed an embedded FAT32 application on Microblaze processor and Files were accessed from SD card through the SD controller.

**Deliverables:**

- Verilog RTL source code
- Test benches
- Synthesis and Simulation scripts
- Detailed user documentation, including RTL

