

Data sheet for BPSK/QPSK/8PSK Demodulator

Introduction:

Phase Shift Keying is a digital modulation scheme that conveys data by changing, or modulating, the phase of a reference carrier signal.

Any digital modulation scheme uses a finite number of distinct signals to represent digital data. PSK uses a finite number of phases, each assigned a unique pattern of binary bits. Usually, each phase encodes an equal number of bits. Each pattern of bits forms the symbol that is represented by the particular phase. The demodulator which is designed specifically for the symbol-set used by the modulator, determines the phase of the received signal and maps it back to the symbol it represents, thus recovering the original data

BPSK, QPSK and 8PSK are three major Modulation Techniques used in most of the applications.

Functional Description:

The Demodulator performs carrier recovery using Costas loop and Symbol Timing Recovery using Early Late gate Algorithm. The QPSK Demodulator accepts 10 bit digital data input from the two ADC's and performs Complex Sine/Cosine multiplication on the Input data. Further it performs Square Root raised cosine filtering with the desired Roll-off factor. The Symbol Timing

recovery is performed with the Matched Filter and Early late Gate Algorithm. Carrier Recovery is performed with Costas loop which Consist of Multiplier and Subtractor Block, Loop Filter and NCO. The In-phase and quadrature outputs are mapped using the De-mapper based on the selected modulation.

Features:

- DVB compliant QPSK/BPSK/8PSK Coherent Demodulator.
- Square Root of Raised Cosine Filtering with Roll-Off: 35%, 25%, 20%.
- Carrier Recovery using "Costas Loop"
- Symbol Timing Recovery using "Early late gate Algorithm"
- Synchronous design
- Programmable Sampling Rates
- Second Order Loop Filters for Carrier Recovery
- Accepts the digital data from two ADC's as input and outputs the demodulated data bits.
- Available for Xilinx FPGA and ASIC implementation.
- Compatible, flexible and easy integration with other modules.

Block Diagram:

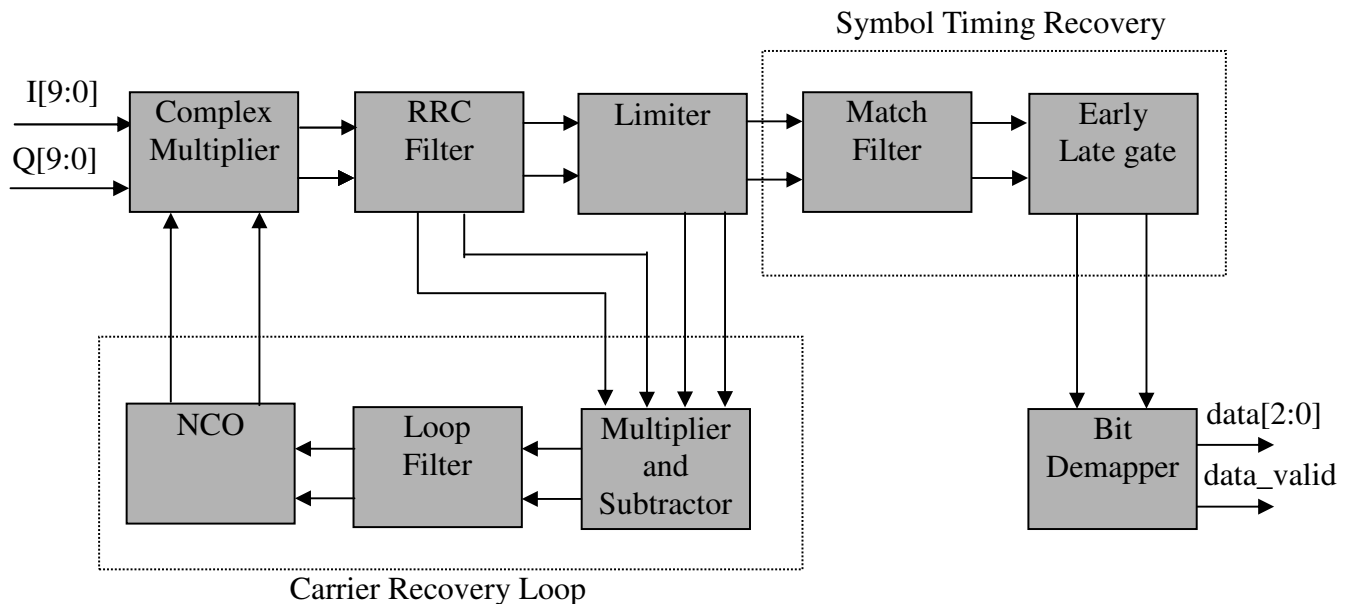


Figure 1: BPSK/QPSK/8PSK Demodulator Block Diagram

Description:

The Fig.1 shows block diagram of QPSK/BPSK/8PSK Demodulator. The detailed description of the Functional blocks are given below

Complex Multiplier:-

The inputs to the device are 10 bit I and Q digital signals. The A/D output data is fed into the Complex Multiplier which performs the Sine and Cosine Multiplication on the input signals. The Sine and Cosine values for Complex Multiplication are taken from the Sine/Cosine table using NCO.

Root Raised Cosine Filter:-

The I and Q symbols produced in this loop are further processed by a Square Root Raised Cosine Filter with programmable Roll-Off factors 0.20,0,25 and 0.35. the Filter removes the high frequency Components present at the input.

Limiter:-

The Limiter is the Amplitude Limiter. The output of the RRC Filter is limited to certain voltage values.

Symbol Timing Recovery:-

Symbol Timing Recovery is done with the help of Matched Filtering and Early Late gate Algorithm. Symbol Timing Acquisition is done with help of matched Filter and Symbol timing Tracking is done using Early late gate Algorithm.

Carrier Recovery:-

Carrier Recovery is done using Costas Loop. It includes Multiplier and subtractor Block which performs operations on Filter and Limiter outputs. The Loop Filter used here is the Second Order FIR Filter. The phase difference is properly adjusted using NCO with the proper Phase shifting in the Look up table.

Bit De-mapper:-

Bit De-mapper maps the demodulated data into bits based on the Modulation type whether BPSK, QPSK or 8PSK. The BPSK outputs 1 bits/symbol, QPSK 2bits/symbol and 8PSK 3 bits per symbol.

Schematic Symbol

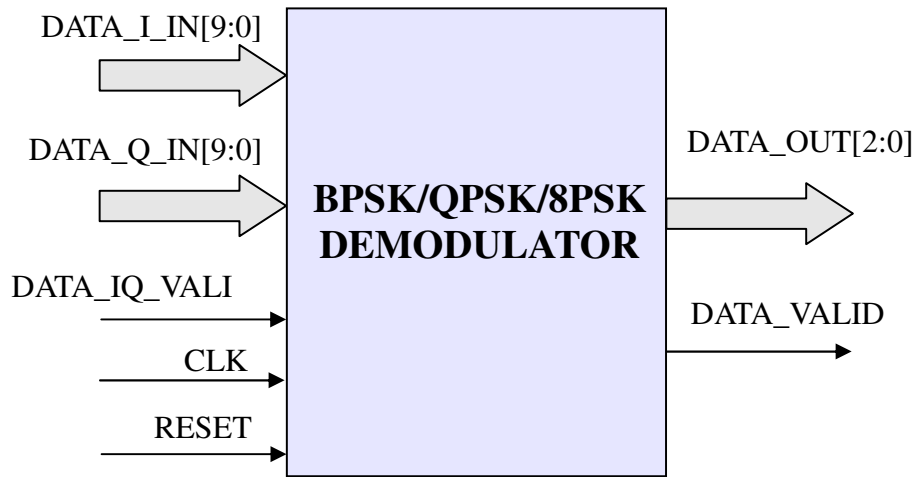


Figure 2: BPSK/QPSK/8PSK Demodulator Schematic Diagram

Signal definition table:

Signal	Direction	Data width	Description
CLK	IN	1	This QPSK clock is single clock system and all I/Os and internal decoder processor is in synchronous with it.
RESET	IN	1	This signal resets the system whenever it is enabled and all counters, registers are sets to starting point.
DATA_I_IN	IN	10	In-phase component 10 bit digital input from ADC
DATA_Q_IN	IN	10	Quadrature component 10 bit digital input from ADC
DATA_IQ_VALID	IN	1	Data valid input signal which indicates the start of data transmission from two ADC's
DATA_OUT	OUT	1/2/3	Demodulated data bits
DATA_VALID	OUT	1	This valid signal indicates the valid output on DATA_OUT line

Table 1: Demodulator signal definition table

Verification:

The QPSK/BPSK/8PSK demodulator core module has been verified with Exhaustive Functional and Timing simulation.

Deliverables:

- Verilog RTL source code
- Test benches
- Synthesis and Simulation scripts.
- Detailed user documentation, including RTL source code documentation.