

## Data sheet for BPSK/QPSK/8PSK/16APSK/32APSK Modulator

### Introduction:

Phase Shift Keying is a digital modulation scheme that conveys data by changing, or modulating, the phase of a reference carrier signal.

Any digital modulation scheme uses a finite number of distinct signals to represent digital data. PSK uses a finite number of phases, each assigned a unique pattern of binary bits. Usually, each phase encodes an equal number of bits. Each pattern of bits forms the symbol that is represented by the particular phase.

BPSK, QPSK, 8PSK, 16PSK, 32PSK are four major Modulation Techniques used in most of the applications.

### Functional Description:

The PSK Modulator designed supports four types of modulation schemes BPSK, QPSK, 8PSK, 16APSK and 32APSK. It has four major Functional blocks. Mapper maps the incoming data bits into I and Q constellation. The FIR Filter performs low pass

filtering of the input I and Q samples to reduce inter-symbol interference. Interpolation filters provide low frequency response characteristics. Finally the Digital Direct Synthesizer performs Sine and Cosine Multiplication on the input I and Q data.

### Features:

- High speed PSK Modulator.
- Four Modulation schemes BPSK, QPSK, 8PSK, 16APSK, 32APSK.
- FIR filter is the Square root Raised Cosine filter with Roll-Off 25%
- Bandwidth Limitation factor for Interpolation Filter is 50%
- Synchronous design
- Available for Xilinx FPGA and ASIC implementation.
- Compatible, flexible and easy integration with other modules.

### Block Diagram:

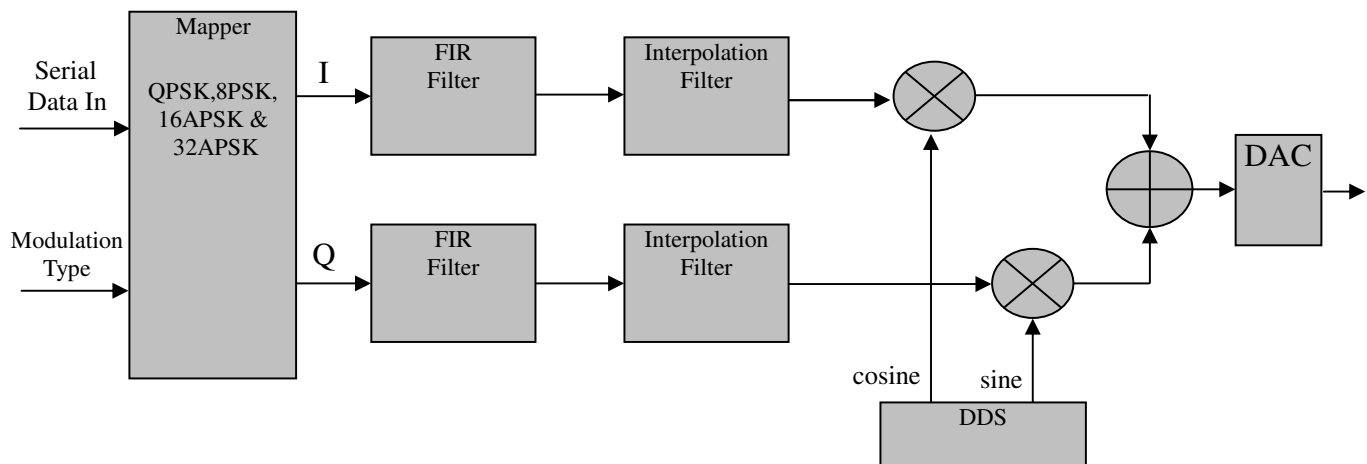


Figure 1: QPSK/8PSK/16APSK/32APSK Modulator Block Diagram

**Description:**

The Fig.1 shows the block diagram of PSK Modulator. The detailed description of the Functional blocks are given below

Mapper:-

Mapper Block maps the input data bits into constellation based on the Modulation type chosen. The output of the Mapper will be In-phase and quadrature components which will be further processed.

FIR Filter:-

The I and Q data paths of the modulator, each contains a pulse shaping filter. Each is 30 tap FIR Filter. They are used to provide bandwidth containment and pulse shaping of the data in order to minimize inter-symbol interference. The filter co-efficients are programmable.

Interpolation Filter:-

The Modulator employs two stages of interpolation

filters in each of the I and Q channels. The interpolation filters not only provide a low frequency response characteristic but also provide the ability to have one sampling rate at the input and another sampling rate at the output.

Mixers and Adders:-

The output of the interpolation filters, the pulse shaped, up sampled I and Q baseband data is multiplied with digitized quadrature version of the carrier cosine and sine values which are provided by the Direct digital Synthesizer (DDS) block. The multiplier outputs are than summed to form PSK Modulated outputs.

**Schematic**

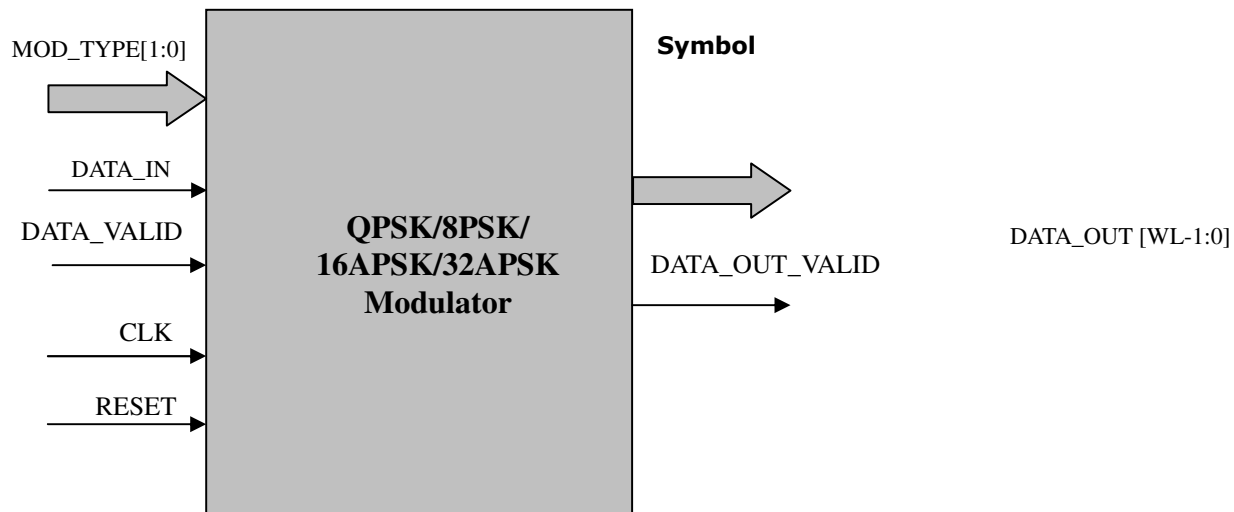


Figure 2: QPSK/8PSK/16APSK/32APSK Schematic Diagram

Signal definition table:

<b>Signal</b>	<b>Direction</b>	<b>Data width</b>	<b>Description</b>
CLK	IN	1	This PSK Modulator clock is single clock system and all I/Os and internal decoder processor is in synchronous with it.
RESET	IN	1	This signal resets the system whenever it is enabled and all counters, registers are sets to starting point.
DATA_IN	IN	1	Serial data input to the PSK Modulator
DATA_IN_VALID	IN	1	Data valid input signal which indicates the valid data at DATA_IN line
DATA_OUT	OUT	WL	Data Output from the Modulator which is given to ADC
DATA_OUT_VALID	OUT	1	Data valid output signal which indicates the valid data at DATA_OUT line

Table 2: QPSK/8PSK/16APSK/32APSK Modulator signal definition table.

**Verification:**

The QPSK/8PSK/16APSK/32APSK demodulator core module has been verified with following approaches:

- Exhaustive Functional/Timing simulation.
- Results compared with MATLAB functions

**Deliverables:**

- Verilog RTL source code
- Test benches
- Synthesis and Simulation scripts.
- Detailed user documentation, including RTL source code documentation.