

## Datasheet for PS/2 Keyboard Interface

### Functional Description

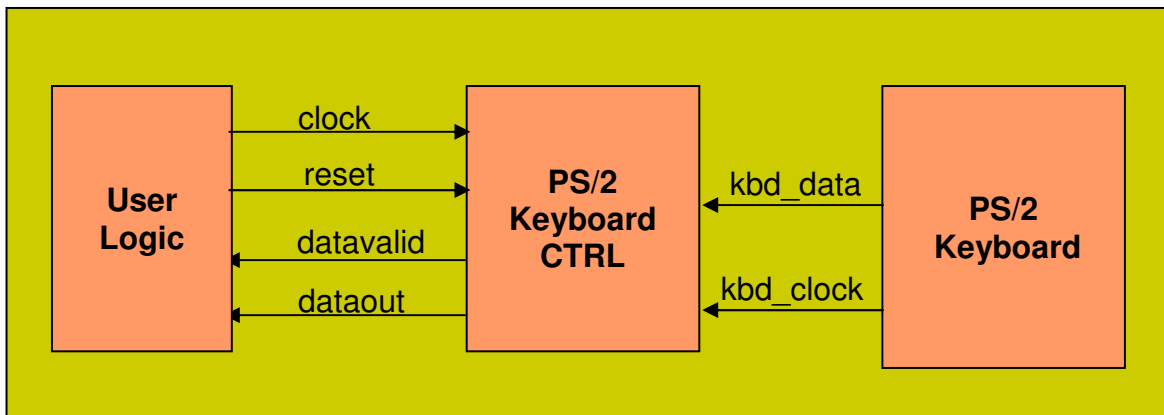
The PS/2 interface is a bit serial interface with two signals Data and Clock. Whenever data and clock line is not in use, both lines are set to logic-1. Block diagram shown below depict the interface between PS/2 peripheral and FPGA. When PS/2 device send data, logic0 is send on kbd\_data and kbd\_clock lines. FPGA detects start of data frame and captured

data bits and parity bit.

### Features:

- Fully synchronize design.
- Parity bit is verified with received data.
- PS/2 clock filter logic.
- Support key combinations with shift key.

### FPGA/PS2 Interface Block Diagram:



### Signal Description

Signal Name	Signal Width	Description
clock	1	This is a input signal and is connected to system clock. This clock is used to drive the controller logic.
reset	1	This input signal is connected to master reset.
kbd_data	1	This input signal is connected to serial data line of the keyboard.
kbd_clock	1	This input signal is connected to clock pin from the keyboard.
dataout	8	This is a output signal from the controller. This is an ASCII equivalent of the scan code received from keyboard.
datavalid	1	This is the output signal from the controller. This signal goes high when valid data is present on the data bus.

**Performance:**

Device	Slice Count	Frequency
Spartan-3A (xc3s700a-4fg484)	108	138 MHz
Virtex-4 (xc4vlx25-11ff668)	119	289 MHz

**Verification:**

The PS/2 Keyboard Interface module has been verified with following approaches:

- Exhaustive Functional/Timing simulation
- Prototyped on Xilinx Spartan-3A and Virtex-4 development board.

**Deliverables:**

- Verilog RTL source code
- Test benches
- Synthesis and Simulation scripts
- Detailed user documentation, including RTL source code documentation