PAL/NTSC Video Encoder

Functional Description

PAL (Phase Alternating Line) and NTSC (National Television System Committee) are encoding systems commonly used in television systems worldwide. PAL mostly used by Western European countries has a frequency of 50 Hz (625-line/50Hz) where as NTSC mostly used by US, Japan and other Asian countries has a frequency of 60Hz (525-line/60Hz).

Both PAL and NTSC work on the same basic principle where color information is amplitude modulated by a subcarrier and luminance information along with synchronization signals are added to generate composite video signal.

Features:

- Supports BT601 and BT656 input formats
- Supports NTSC(M), PAL(B,D,G,H,I), PAL (M) and PAL(N) output video standards
- Supports RGB, YUV, S-Video and Composite output video formats
- Supports Color Bar mode
- Supports Ancillary data (WSS and CGMS)
- Programmable Luma and Chroma filters
- Programmable Luma delay
- APB Interface to Register Set
- Supports Vertical Blanking Interval (VBI) encoding support including closed caption, teletext, WSS & CGMS Encoding

Block Diagram:

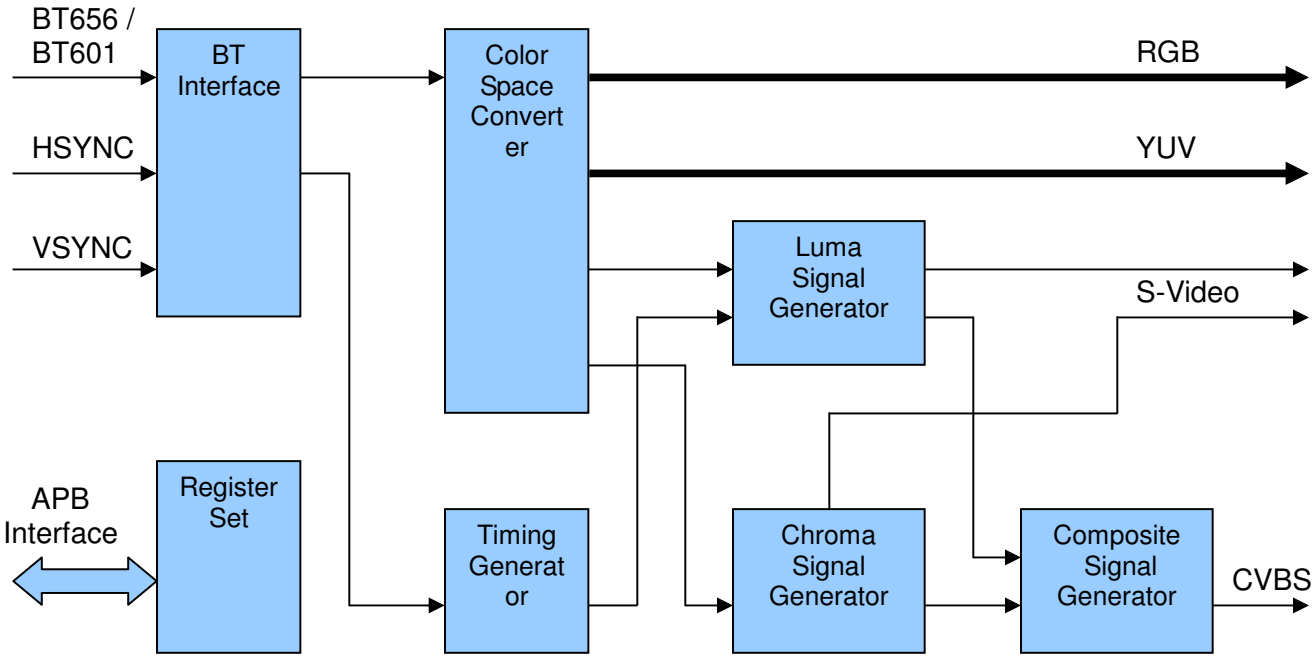

Figure 1: Digital Video Encoder

Description:

Digital Video Encoder converts 8-bit digital BT601/BT656 4:2:2 signal to 10-bit standard digital composite video signal.

Following is a brief description of the different blocks in Video Encoder:

BT Interface: This module accepts 8-bit YcbCr data in BT656/601 format and performs necessary processing to handover raw pixel data to Color Converter module. Some of the functions performed by this module are: detecting start of frame, extracting timing information and auxiliary data.

Color Space Converter: Color Space Converter receives raw pixel data and converts it to different formats for supporting different output formats.

Timing Generator: This block is responsible for generating synchronizing pulses essential for PAL, & NTSC standards.

Luma Signal Generator: Programmable luma filtering and delaying is performed by this module in addition to luma processing. Auxiliary data is also processed by this module.

Chroma Signal Generator: This block modulates chroma information on to subcarrier to generate modulated chroma signal. It also provides a facility for programmable chroma filter.

Composite Signal Generator: This block generates composite signal by combining processed luma signal and modulated chroma signal.

Register Set: All the programmable parameters of the Video Encoder can be controlled by writing to appropriate registers. User can access these registers through an APB Interface.

Signal definition table:

Signal Name	***Direction***	***Description***
CLK	Input	54 MHz clock
BT_D[7:0]	Input	Video data input in BT601 or BT656 format.
BT_HSYNC	Input	Horizontal Sync Signal.
BT_VSYNC	Input	Vertical Sync Signal.
DAC0[9:0]	Output	Output going to DAC0.
DAC1[9:0]	Output	Output going to DAC1.
DAC2[9:0]	Output	Output going to DAC2.
DAC3[9:0]	Output	Output going to DAC3.
DAC_PD[3:0]	Output	Power up/down for individual DAC, Read from registers
PSEL	Input	Select Signal, which is active during transaction.
PENABLE	Input	Enable indicating the start of transaction.

Signal Name	Direction	Description
PWRITE	Input	Write transaction when active, else read transaction.
PADDR[13:0]	Input	Register address.
PWDATA[31:0]	Input	Data to register set.
PRDATA[31:0]	Output	Data from register set.
PRESET_N	Input	Active low reset.

Schematic Symbol:

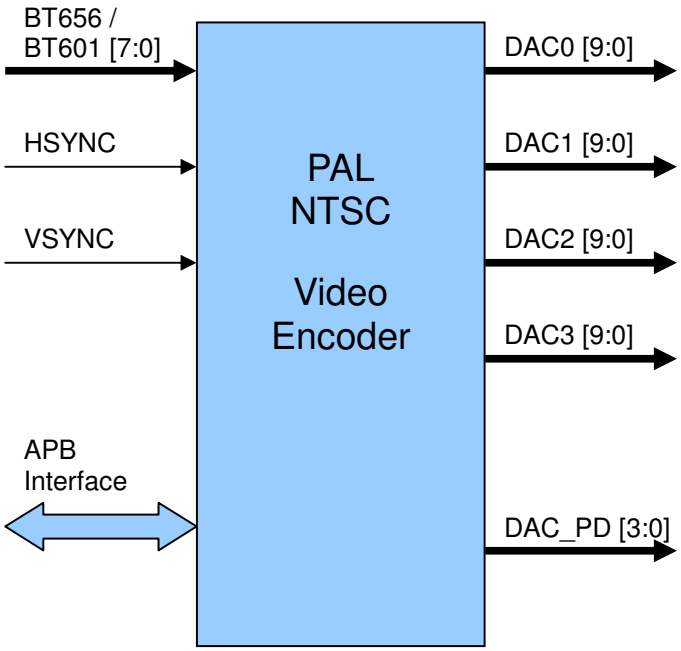

Figure 2: Schematic Symbol

Typical Application:

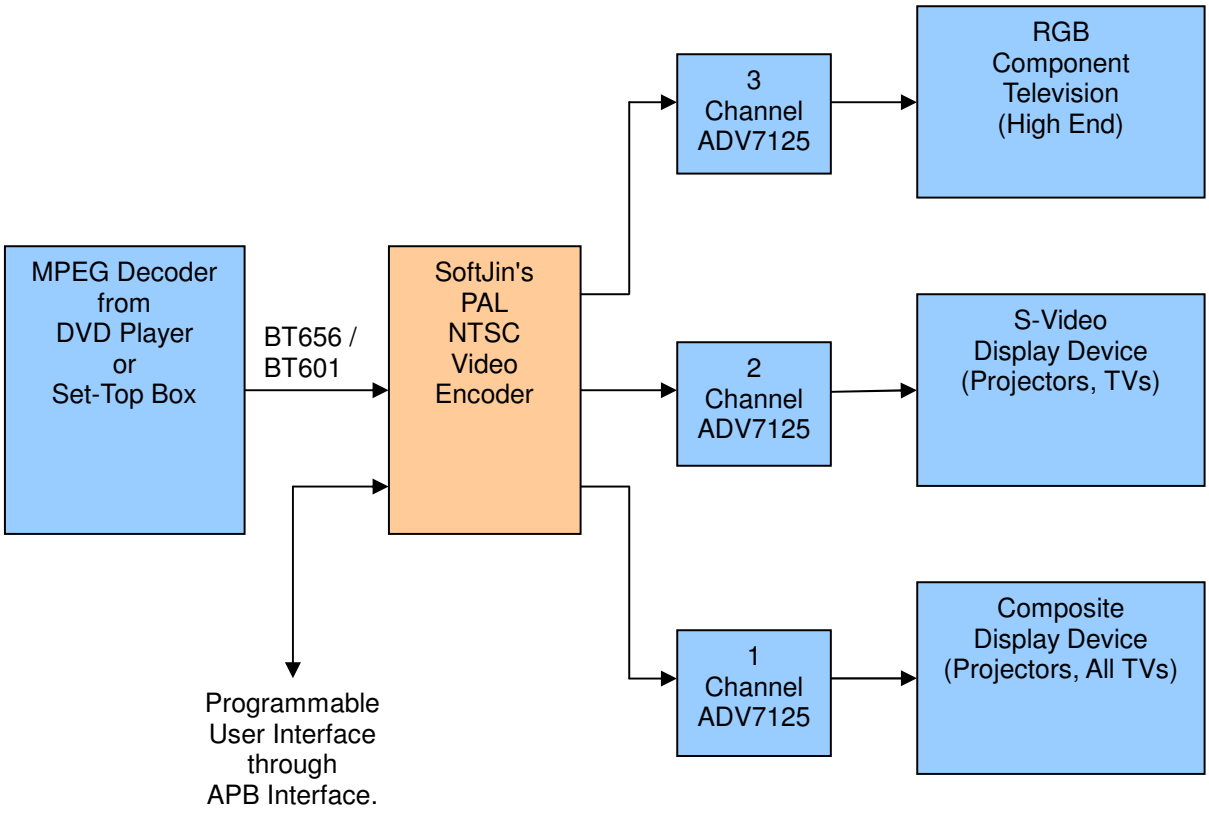

Figure 3: Typical Application Diagram

Performance:

Device	Slice Count	Frequency
Virtex-4 (xc4vlx25-12ff668)	16338	60 MHz

Register Set:

The user programmable registers are grouped in different categories, which include control registers, subcarrier registers, coefficient registers and data registers. All registers are 32-bit wide and can be accessed through APB interface.

Some of the parameters that can be controlled are

- Input and output standards
- Support for Auxiliary data
- Filter types
- Conversion coefficients

Verification:

The PAL-NTSC Video Encoder modules have been verified with following approaches:

- Simulations using Xilinx ISE and Mentor's Modelsim.
- Prototyped on Xilinx ML401 Board and viewed on LCD TV, NEC Projector.