

## Data sheet for NAND FLASH Controller

### Functional Description

SoftJin's NAND FLASH controller IP provides easy interface for user to communicate with NAND FLASH device. The controller has a very flexible FIFO like interface for storing and retrieving data from NAND flash. Controller has simple memory mapped interface to configure the controller registers and in turn to carry out NAND operations

### Key Features

- IP core is compliant with the Open NAND Flash Interface Working Group (ONFI) 1.0 standard.
- Supports asynchronous SLC and MLC NAND flash devices from leading NAND manufacturers -Micron, Samsung, Numonyx etc.
- Fully parameterizable controller, to cater different timing for different devices and timing modes.
- Supports timeout mechanism for all the controller and NAND operations
- Interrupt to notify completion of an operation and status of operation

### ECC support (Optional)

- Hamming: 1 bit correctability in 256 bytes of data
- BCH: Up to 16 bits correctability in 1024 bytes of data.

### Rich Command set:

- Initialize / reinitialize
- Read single page , read multiple pages
- Program single page , program multiple pages
- Erase blocks
- Copy-back feature to do internal copying of a page in NAND flash
- Get/set features of flash
- Read parameter page from flash

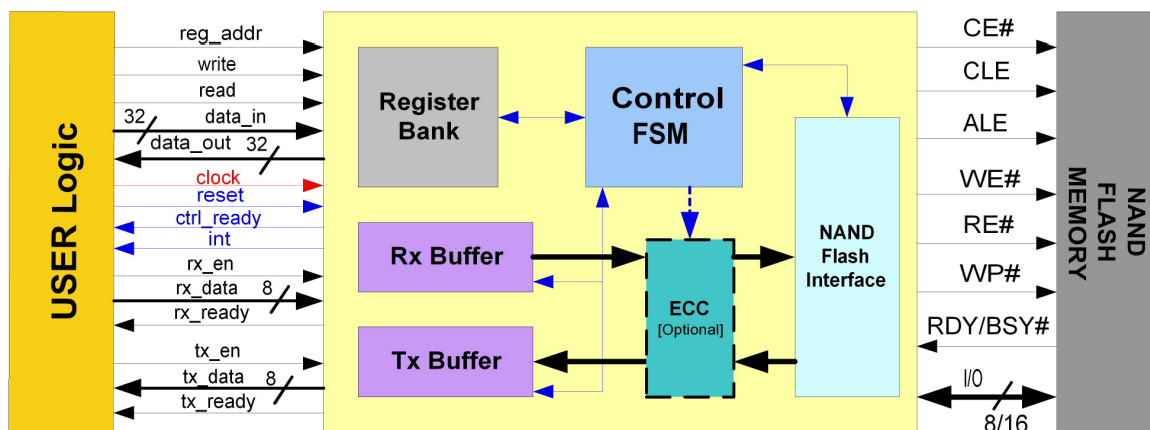
### Configurable Parameters

- Configurable timing parameter registers to aid operating in various timing modes supported by flash device.
- Timing parameters include controlling pulse widths of NAND flash control signals.
- Page size of NAND device

### Bypass Mode:

- Supports bypass mode / non interpretation mode where host can send actual commands. Controller only manages protocol and timing requirements.
- Write address , with configurable number of address cycles
- Write command
- Write data with number of bytes/words to be transferred to flash
- Receive data, with number of bytes/words to be received from flash

### Block Diagram:



### Pin Description:

User Logic Interface Signals		
I/O Name	Width	Description
Clock	1	Board clock input to the controller module.
Reset	1	Asynchronous active high reset for controller module.
Reg_addr	3	Address input to access the register bank.
Data_in	32	Data input to the register bank.
Data_out	32	Data output from the register bank.
Read	1	Active high read enable for register bank.
Write	1	Active high write enable for register bank.
Rx_data	8	data input to the RX buffer.
Tx_data	8	data output from TX buffer.
Rx_en	1	write enable for RX buffer.
Tx_en	1	read enable for TX buffer.
Rx_ready	1	On active high Rx buffer is ready to receive data.
TX_ready	1	On active high TX buffer is ready to send data.
Int	1	Interrupt line to convey operation over to host

NAND Flash Interface Signals		
I/O Name	Width	Description
CE#	1	Active low chip enable to NAND.
CLE	1	Command latch enable pin on NAND.
ALE	1	Address latch enable pin on NAND.
WE#	1	Write enable pin of NAND.
RE#	1	Read enable pin of NAND.
WP#	1	Write Protect pin of NAND.
I/O bus	8 or 16	Multiplexed IO bus for data, command, address
R/B#	1	Active high ready or Active low busy.



Figure 1 NAND Flash Eval Board

### Verification:

The NAND Flash controller module has been verified with following approaches:

- Exhaustive Functional/Timing simulation using a NAND Flash behavioral model.(ONFi 1.0)
- On-board testing with SoftJin’s NAND FLASH evaluation board (Figure 1) interfaced with off the shelf Spartan-6 and Virtex 5 FPGA boards
- Eval board has Micron (**29F2G08AAD**) and ST Microelectronics (**NAND01GW3B**) SLC NAND Flash parts

### Performance Numbers

IP Configuration	NAND Device	Page program Throughput (M Bytes/ sec)	Page Read Throughput (M Bytes/ sec)	
			With Errors	Without Errors
NAND Flash Controller [No ECC]	Micron: <b>29F2G08AAD</b>	6.5	23.63	
NAND Flash Controller [Hamming ECC]		6.43	21.61	22.79
NAND Flash Controller [BCH ECC]	ST Microelectronics <b>NAND01GW3B</b>	4.43	1.8	4.57

### Recourse Utilization

IP Configuration	No ECC			Hamming ECC			BCH ECC		
	Slice Registers	LUTs	BRAMs	Slice Registers	LUTs	BRAMs	Slice Registers	LUTs	BRAMs
<b>Spartan6</b>	889	929	4	1301	1421	13	5442	9701	30
<b>Virtex 5</b>	945	886	2	1365	1463	7	5419	9756	16

### Deliverables:

- Verilog RTL source code and source code documentation
- Test benches
- Synthesis and Simulation scripts
- Detailed user documentation,