

Data sheet for Matrix Multiplication Core

Introduction:

Matrix multiplication is a basic manipulation of matrices, used in wide spread applications like communication, image, audio and video encoder and decoders etc.

Features:

- High speed matrix multiplication algorithm.
- Compatible with all code and data lengths.
- Synchronous design.

- Provision to change order of matrices dynamically.
- Available for Xilinx FPGA and ASIC implementation.
- Core can be configured for any order of matrix.
- Area and power optimized implementation
- Compatible, flexible and easy integration with other modules.
- Low latency and high throughput.

Block Diagram:

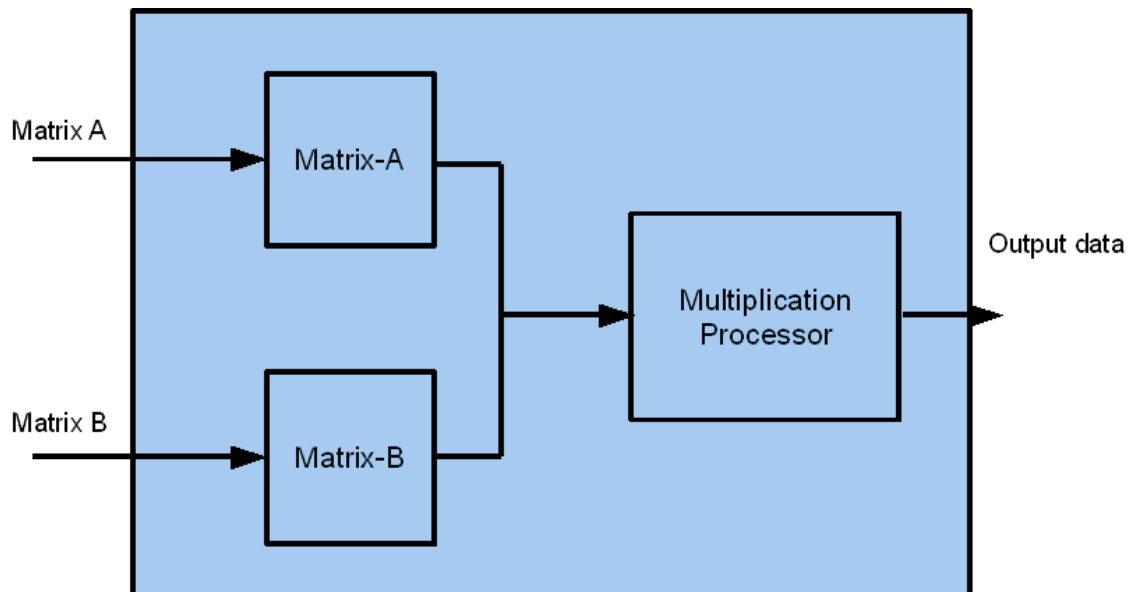


Figure 1: Matrix Multiplier Block Diagram

Description:

1. The Figure 1 shows block diagram of Matrix multiplier.
2. Two matrices to be multiplied are stored in Matrix-A and Matrix-B RAMs respectively.
3. These two matrices are given to Multiplication processor, where our high speed algorithm computes multiplication of these two matrices

and gives out.

4. Table.1 lists out all parameters used in the core and are detailed.
5. Figure 2 shows the schematic symbol of the IP core and all input and output ports have been represented with their data width.
6. Table.2 shows all input and output signal

declarations, along with their type, width and detail explanations have been given.

7. Table.3 shows the performance of the IP core when targeted on virtex-4 and virtex-5 families.

Parameters:

This table describes the general Matrix Multiplier parameters:

Parameter	Type	Description
WL	Integer	Represents width of the each data symbol.
IWL1	Integer	Represents width of the integer part of input data at input port i_datain_A
IWL2	Integer	Represents width of the integer part of input data at input port i_datain_B
IWL	Integer	Represents width of the integer part of output data at output port o_multiply_out
COUNT_A	Integer	Represents the width of address which is used to address input matrix A.
COUNT_B	Integer	Represents the width of address which is used to address input matrix B.

Table 1: Matrix Multiplier Parameter table.

Schematic Symbol

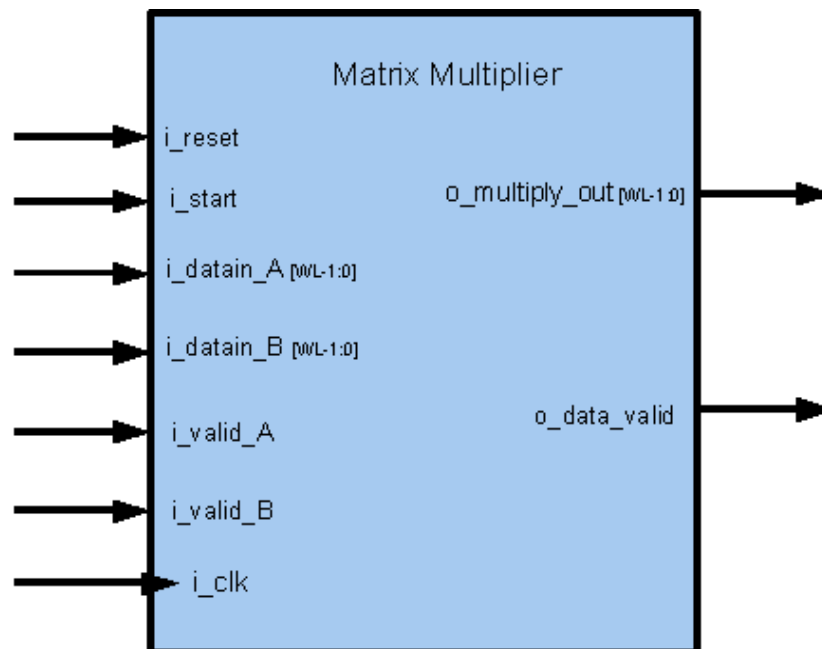


Figure 2: Matrix Multiplier Schematic Diagram

Signal definition table:

Signal	Direction	Data width	Description
i_clk	IN	1	Matrix Multiplier is a single clock system and all I/Os and internal multiplier processor is in synchronous with it.
i_reset	IN	1	This signal resets the system whenever it is enabled and all counters, registers are sets to starting point.
i_start	IN	1	Single bit input signal which starts the multiplier processor.
i_datain_A	IN	WL	This is input port of WL data width through which input matrix-A data is fed through.
i_datain_B	IN	1	This is input port of WL data width through which input matrix-B data is fed through.
i_valid_A	IN	1	Single bit input signal which when enabled indicates that the data input at port i_datain_A is valid input to core.
i_valid_B	IN	1	Single bit input signal which when enabled indicates that the data input at port i_datain_B is valid input to core.
o_data_valid	OUT	1	Single bit output port which when enabled indicates that data presented at output port is valid.
o_multiply_out	OUT	WL	Output port of width WL, through which computed data will be given out.

Table 2: Matrix Multiplier signal definition table.

Performance:

Device	Slice Count	Frequency (MHz)
Virtex-4	183	168
Virtex-5	94	192

Table 3: Matrix Multiplier Core performance table.

Verification:

The Matrix Multiplication core module has been verified with following approaches:

- Exhaustive Functional/Timing simulation.
- Results compared with MATLAB functions and Matrix Multiplication -C code functionality.

Deliverables:

- Verilog RTL source code
- The IP core test environment developed in verilog HDL (test benches).
- Synthesis and Simulation scripts.

- Detailed user documentation, including RTL source code documentation.
- Architecture specification.

Applications:

1. Telecommunications.
2. Image Encoder/Decoders.
3. Audio Encoder/Decoders.
4. Video Encoder/Decoders.
5. Computer graphic chips.
6. DSP chips found in cell phones and digital cameras.