

LDPC Encoder for DVBS2

Introduction:

The LDPC Encoder core provides designers an LDPC Encoder block used in DVB-S2 systems.

LDPC codes are the codes that offers error detection and correction capabilities close to maximum theoretical limits. LDPC codes were discovered by Gallager in 1962. But they were not given much attention for decades as the technology was not matured enough for its efficient implementation. With the success of iterative 'turbo codes' MacKay and Neal reintroduced LDPC codes in 1995.

LDPC codes have easily parallelizable encoding and decoding algorithms. The parallelizability is 'adjustable' providing the user an option to choose between throughput and complexity.

The function of the encoder is to add extra redundant data for given uncoded data. This extra redundant data, called as parity data is useful in detecting the errors that are introduced during the data transmission through a channel. LDPC encoder along with BCH encoder block is used for generating the parity data in DVB-S2 systems.

DVB-S2 is the second-generation for satellite broad-band applications, developed by Digital Video Broadcasting (DVB) Project in 2003. This is the first standard that uses LDPC mechanism for error detection and correction. It's a single and very flexible standard that covers variety of satellite broadcasting applications. This system also have it's applications in interactive services, professional applications such as digital TV contribution, news gathering, data content distribution and Internet trunking.

Features :

- High speed DVB-S2 LDPC encoder
- Compliant with DVB-S2 standard
- Supports both normal(64800) and short(16400) Frame lengths
- Supports all code rates for long frame(1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6,8/9,9/10).
- Supported code rates for short frame (1/3,3/5,2/3,8/9)
- Optimized for speed and area.
- Easy to integrate with other modules.
- Fully synchronous design with single clock.

Description :

The LDPC Encoder core is compliant to DVB_S2 standard.

For generating parity bits the DVB-S2 system has a fixed set of parity equations for a given code rate. The DVB-S2 LDPC encoder core generates the parity data by using the parity equations that are provided by the DVB-S2 standard.

The process of encoding starts by initializing every parity bit to zero. Then from the parity generator matrix provided by the standard obtain the addresses of information bits that need to be ex-ored . Ex-Or the information bits at those locations to generate the parity bit. The final parity bits are generated by ex-oring every parity bit with the previous parity bit.

LDPC codes for DVB-S2 have the property of repeatability. The addresses of information messages are in a periodic fashion. So there is no need to save the address values for every parity bit. This reduces the memory requirement by a factor 360.

Functionality :

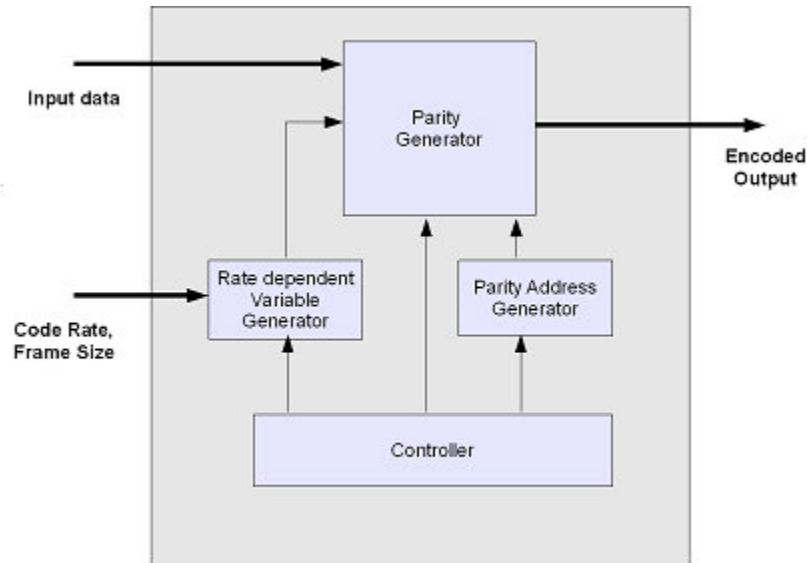


Figure1 : Functional Diagram

Parameter Table :

Parameter	Type	Description
input_wl	Integer	Represents the word length of input

Table 1: LDPC Encoder parameter table.

User Interface:

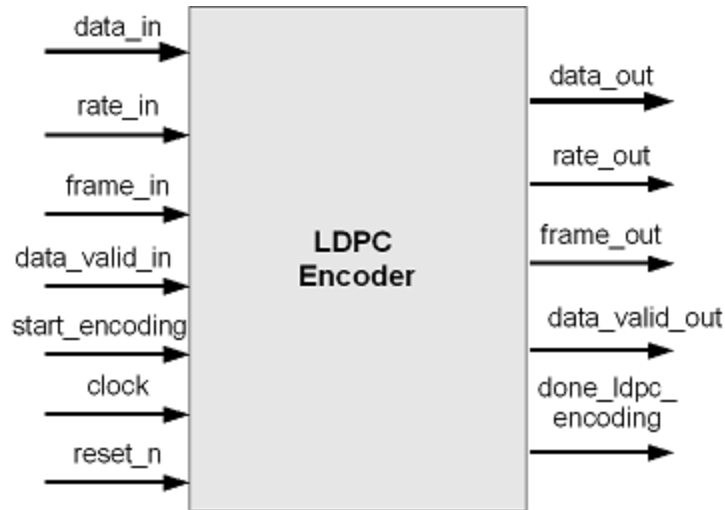


Figure2 : Schematic Block Diagram

Pin Description :

Signal	Direction	Data Width	Description
clock	Input	1	Global synchronous clock
reset_n	Input	1	Active Low Reset
data_in	Input	input_wl	Input Data
rate_in	Input	4	Rate selector
frame_in	Input	1	Frame Selector 1 = normal frame(64800) 0 = short frame (16200)
data_valid_in	Input	1	Set to be high when data at input 'data_ip' is valid
start_encoding	Input	1	Start encoding signal
done_ldpc_encoding	Output	1	Signal indicating end of encoding
data_valid_out	Output	1	Set high by core, when data at output data_op is valid
frame_out	Output	1	Frame Identification for current output frame
rate_out	Output	4	Rate Identification for current output frame
data_out	Output	input_wl	Output Data

Table 2: Signal Definition Table

Code Rates :

rate_in	1	2	3	4	5	6	7	8	9	10	11
Code Rate	'1/4'	'1/3'	'2/5'	'1/2'	'3/5'	'2/3'	'3/4'	'4/5'	'5/6'	'8/9'	'9/10'

Table 3: Valid Values for Code Rate

Figure 1. shows the main blocks of the DVB-S2 LDPC Encoder unit. The LDPC encoder receives code rate, frame size along with the data that need to be encoded as inputs.

LDPC Encoder has three main functional blocks. Rate dependent variable generator, Parity address generator and parity generator.

For a given code rate and frame size, rate dependent variable generator block generates the values information bit length, parity bit length and repeatability rate which are used in encoding.

Parity address generator contains the address of information bits that need to be ex-ored for generating a given parity bit.

Parity generator receives the information bits from input and address values from parity address generator block to generate the parity data.

Figure 2. shows the schematic block diagram of LDPC Encoder core. Table 2. gives the description of pins of core. Rate and frame size can be changed on a frame to frame basis.

With the assertion of start encoding signal, the encoder starts receiving the uncoded data from data_in pin at a rate mentioned by the user. Encoder receives data only when data_valid_in pin is set to high. Once the complete frame is

received, decoder starts encoding process. Rate and frame size values provided from the pins rate_in and frame_in are used for selecting the address of parity bits and other variables that are used in the encoding process. Using these values the parity generator starts generating parity bits.

Once parity bits are generated the core asserts done_ldpc_encoding signal. Parity bits are generated at intervals of parity repeat rate provided by the standard. For example in code rate 1/2, repeat rate is 90. So parity bits at locations 0,90,180.. are generated. The encoded data along with transmitted data is sent out from pin data_out at a user specified rate. data_valid_out pin is set to high when the output data at the data_out pin is valid. rate_out and frame_out are the rate and frame size indication pins for the current frame.

Table 3 gives the valid rate_in values in decimal format and the corresponding rate it indicates. Table 4 gives the performance values of LDPC Encoder core on virtex 4 and virtex 5 platforms.

Performance :

Device	Flops	LUT's	RAM's	Frequency (MHz)
Virtex-4 (XC4VLX25-10-ff668)	8780	15707	15	115.53
Virtex-5 (XC5VLX30-FF324)	7447	10862	15	167.17

Table 4: LDPC Encoder for DVB-S2 Performance table.

Verification:

- Test Vectors are developed using c-model.
- Results are compared with the C model results for different code rates.

Deliverables:

- C-Model, Verilog RTL source code
- Test Benches
- C-Model code for generation of test vectors
- Detailed user documentation

Applications :

Typical Application of LDPC Encoder is in DVB-S2 for generating parity data. Various other applications include

- Broadcasting of standard definition and high-definition TV (SDTV and HDTV)
- Satellite Communications
- interactive services, including Internet access, for consumer applications
- professional applications, such as digital TV contribution and news gathering
- data content distribution and Internet trunking
- Microwave communications
- cellular backhaul