

Data sheet for JPEG Encoder Core

Functional Description:

The application is a BMP format to JPEG format converter. JPEG is a format used for compression of photographic images. The degree of compression is proportionate to the degree of quantization performed on each image coded unit, and thus can be controlled. This application performs baseline sequential DCT-based JPEG conversion on photographic images

Features:

- Baseline ISO/IEC 10918-1 standard
- 8x8 two dimensional DCT using fixed point
- Configurable Quantization tables
- 8 bit per pixel
- Supports color components in 4:4:4, 4:2:2 and 4:2:0 formats

Block Diagram:

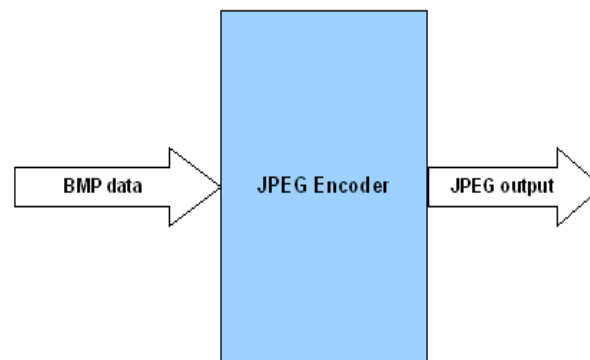


Figure 1: Block Diagram

Architectural Diagram:

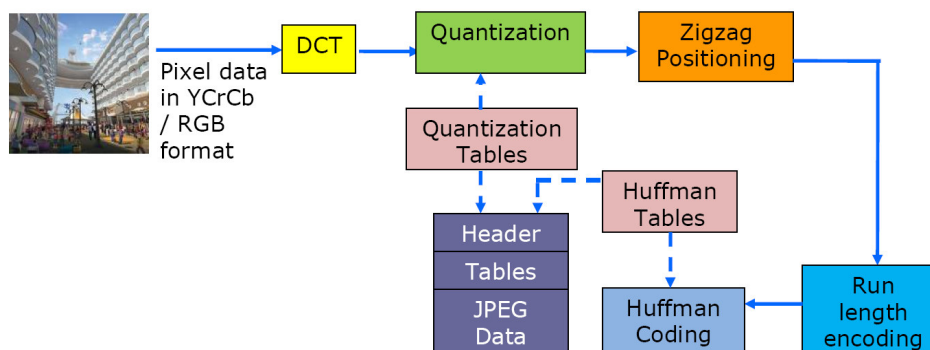


Figure 2: JPEG encoder Architecture Diagram

Description:

1. Initially the quantization tables are filled. There are two quantization tables; for luminance, and for chrominance
2. Whenever a frame is given as input the SOF_IN pulse is given to indicate the start of the frame. For the first and last frames of the

input data, SOI_IN and EOI_IN pulses respectively are given. The signal YCBCR_IN indicates the type of frame .i.e. Y, Cb or Cr frame. Once a frame is started, all the 64 inputs of the frame must be given continuously. The MODE input decides whether the compressed

output is in 4:4:4, 4:2:2 or 4:2:0 format. This is a constant input.

3. Whenever writing into input Ram-A is done, a ready signal `i_READY_A` is given as input.

4. The input DCT section of the IP has a DUAL buffer system, so when one buffer is filled with data, it can start processing, and meanwhile the

other buffer is filled up. Thus when RAM-A is filled, data can be sent to RAM-B while holding the `i_READY_B` signal HIGH.

5. On the output side, the data is received as signal `DATAOUT`. The signal `DATAOUT_VALID` indicates arrival of valid data on the output.

6. The pulses `SOI_OUT` and `EOI_OUT` indicate the start and end of output data.

JPEG Encoder Core Parameter Table

This table describes the important JPEG parameters:

BMP_FILENAME	String	Useful for simulation only. Gives the name and location of the input bitmap file
WIDTH	Integer	Useful for simulation only. Gives the width in pixels of the input bitmap file
HEIGHT	Integer	Useful for simulation only. Gives the height in pixels of the input bitmap file

Signal definition table:

Signal	Direction	Description
<code>i_PIXEL_DATA [7:0]</code>	IN	This is the data input to the module
<code>i_READY_A</code>	IN	This signal indicates that data is to be fed to RAM-A of the Dual buffer
<code>i_READY_B</code>	IN	This signal indicates that data is to be fed to RAM-B of the Dual buffer
<code>WE_COEFF</code>	IN	This the write enable signal for the quantization table memory
<code>DIN_COEFF[7:0]</code>	IN	This is the data input to the quantization table memory
<code>SOF_IN</code>	IN	This is the 'start of frame' signal
<code>SOI_IN</code>	IN	This is the 'start of image' signal
<code>EOI_IN</code>	IN	This is the 'end of image' signal
<code>YCBCR_IN[1:0]</code>	IN	This signal indicates whether the current is a Y, Cb or Cr frame
<code>i_LAST_FRAME</code>	IN	This signal is held high when the last frame is given
<code>MODE[1:0]</code>	IN	This gives the mode of compression 01 - 4:4:4 format 10 - 4:2:2 format 11 - 4:2:0 format
<code>CLOCK</code>	IN	This is the system clock
<code>RESET</code>	IN	This is the system reset
<code>IMAGE_HEIGHT[15:0]</code>	IN	This gives the height of the image in pixels. The value should be a

Signal	Direction	Description
		multiple of 8.
IMAGE_WIDTH[15:0]	IN	This gives the width of the image in pixels. The value should be a multiple of 8.
DATAOUT[7:0]	OUT	This is the data output of the encoder
DATAOUT_VALID	OUT	This indicates whether the data at the output is valid or not
SOI_OUT	OUT	This signal indicates start of JPEG output stream
EOI_OUT	OUT	This signal indicates end of JPEG output stream

Schematic Symbol:

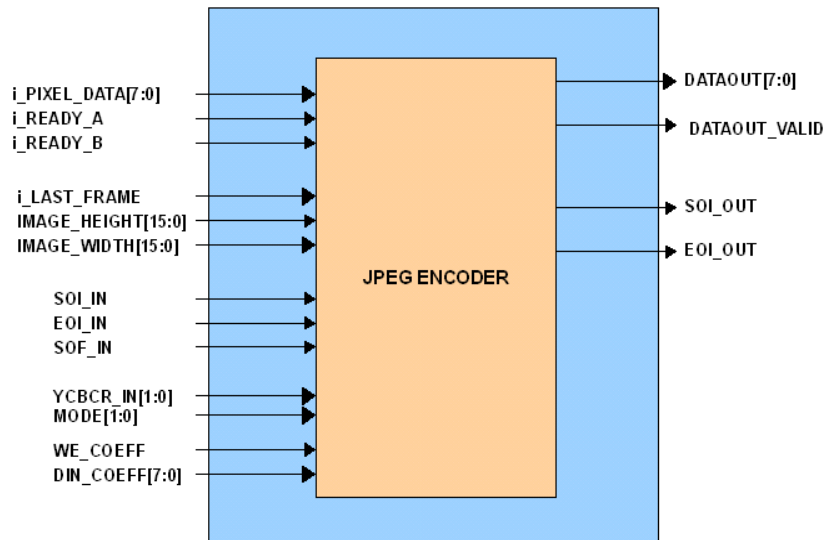


Figure 3: Schematic Symbol

Performance:

Device	Slice LUT Count	Slice Register Count	Frequency
Virtex-4 lx25 -10ff668	5577	2599	66 MHz
Virtex-5 lx50t -3ff1136	4234	2572	136 MHz

Frame Resolution	Time taken per frame by JPEG encoder (at 100 MHz Frequency)
640x480	9.4 ms
720x576	12.6 ms

Verification:

The JPEG Encoder module has been verified with exhaustive Functional/Timing simulation.

Deliverables:

- Verilog RTL source code
- Test benches
- Synthesis and Simulation scripts.
- Detailed user documentation, including RTL source code documentation