

## Data sheet for JPEG Encoder Core

### Functional Description:

The application is a BMP format to JPEG format converter. JPEG is a format used for compression of photographic images. The degree of compression is proportionate to the degree of quantization performed on each image coded unit, and thus can be controlled. This application performs baseline sequential DCT-based JPEG conversion on photographic images

### Features:

- Baseline ISO/IEC 10918-1 standard
- 8x8 two dimensional DCT using fixed point
- Configurable Quantization tables
- 8 bit per pixel
- Supports color components in 4:4:4, 4:2:2 and 4:2:0 formats

### Block Diagram:

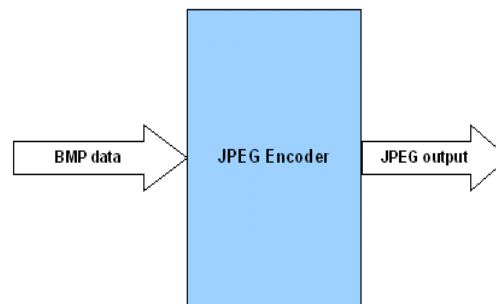


Figure 1: Block Diagram

### Architectural Diagram:

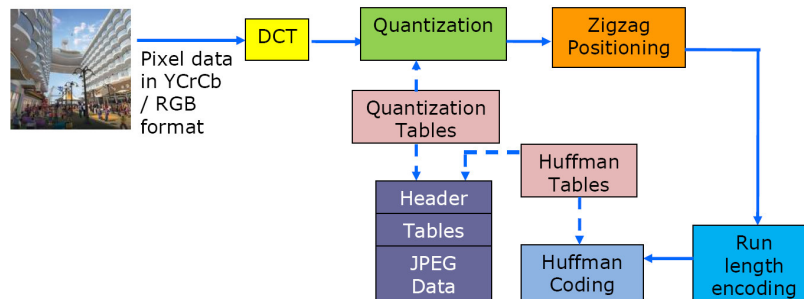


Figure 2: JPEG encoder Architecture Diagram

### Description:

1. Initially the quantization tables are filled. There are two quantization tables; for luminance, and for chrominance
2. Whenever a frame is given as input the SOF\_IN pulse is given to indicate the start of the frame. For the first and last frames of the input data, SOI\_IN and EOI\_IN pulses respectively are given. The signal YBCR\_IN indicates the type of frame .i.e. Y, Cb or Cr frame. Once a frame is started, all the 64 inputs

of the frame must be given continuously. The MODE input decides whether the compressed output is in 4:4:4, 4:2:2 or 4:2:0 format. This is a constant input.

3. Whenever writing into input Ram-A is done, a ready signal i\_READY\_A is given as input.
4. The input DCT section of the IP has a DUAL buffer system, so when one buffer is filled with data, it can start processing, and meanwhile the

other buffer is filled up. Thus when RAM-A is filled, data can be sent to RAM-B while holding the i\_READY\_B signal HIGH.

5. On the output side, the data is received as

signal DATAOUT. The signal DATAOUT\_VALID indicates arrival of valid data on the output.

6. The pulses SOI\_OUT and EOI\_OUT indicate the start and end of output data.

### JPEG Encoder Core Parameter Table

This table describes the important JPEG parameters:

BMP_FILENAME	String	Useful for simulation only. Gives the name and location of the input bitmap file
WIDTH	Integer	Useful for simulation only. Gives the width in pixels of the input bitmap file
HEIGHT	Integer	Useful for simulation only. Gives the height in pixels of the input bitmap file

### Signal definition table:

<b>Signal</b>	<b>Direction</b>	<b>Description</b>
i_PIXEL_DATA [7:0]	IN	This is the data input to the module
i_READY_A	IN	This signal indicates that data is to be fed to RAM-A of the Dual buffer
i_READY_B	IN	This signal indicates that data is to be fed to RAM-B of the Dual buffer
WE_COEFF	IN	This the write enable signal for the quantization table memory
DIN_COEFF[7:0]	IN	This is the data input to the quantization table memory
SOF_IN	IN	This is the 'start of frame' signal
SOI_IN	IN	This is the 'start of image' signal
EOI_IN	IN	This is the 'end of image' signal
YCBCR_IN[1:0]	IN	This signal indicates whether the current is a Y, Cb or Cr frame
i_LAST_FRAME	IN	This signal is held high when the last frame is given
MODE[1:0]	IN	This gives the mode of compression 01 - 4:4:4 format 10 - 4:2:2 format 11 - 4:2:0 format
CLOCK	IN	This is the system clock
RESET	IN	This is the system reset
IMAGE_HEIGHT[15:0]	IN	This gives the height of the image in pixels. The value should be a multiple of 8.
IMAGE_WIDTH[15:0]	IN	This gives the width of the image in pixels. The value should be a multiple of 8.
DATAOUT[7:0]	OUT	This is the data output of the encoder
DATAOUT_VALID	OUT	This indicates whether the data at the output is valid or not

<b>Signal</b>	<b>Direction</b>	<b>Description</b>
SOI_OUT	OUT	This signal indicates start of JPEG output stream
EOI_OUT	OUT	This signal indicates end of JPEG output stream

**Schematic Symbol:**

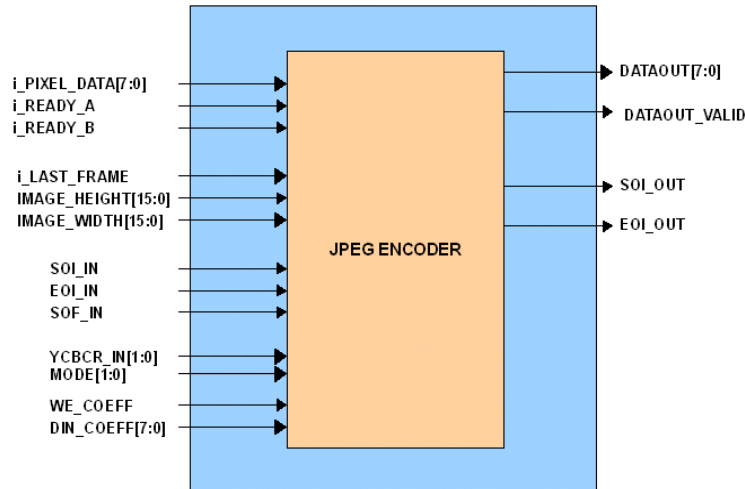


Figure 3: Schematic Symbol

**Performance:**

<b>Device</b>	<b>Slice LUT Count</b>	<b>Slice Register Count</b>	<b>Frequency</b>
Virtex-4 Ix25 -10ff668	5577	2599	66 MHz
Virtex-5 Ix50t -3ff1136	4234	2572	229 MHz

**JPEG Encoder Frame Rate:**

The following table shows possible frame rate with JPEG encoder running on Altera Stratix III or Xilinx Virtex-5 device at 200 MHz.

<b>Image Type</b>	<b>Resolution</b>		<b>Possible Frame Rate Per Sec (At 200 MHz) at different YCbCr format</b>		
	<b>Width</b>	<b>Height</b>	<b>4:2:0</b>	<b>4:2:2</b>	<b>4:4:4</b>
VGA	640	480	370	277	185
NTSC	720	480	329	246	164
PAL	720	576	274	205	137
HD	1280	720	123	92	61
HD	1920	1080	54	41	27

**Verification:**

The JPEG Encoder module has been verified with exhaustive Functional/Timing simulation.

**Deliverables:**

- Verilog RTL source code
- Test benches
- Synthesis and Simulation scripts.
- Detailed user documentation, including RTL source code documentation