

Data sheet for JPEG Decoder Core

Functional Description:

The application is a JPEG format to BMP format converter. JPEG is a format used for compression of photographic images. The degree of compression is proportionate to the degree of quantization performed on each image coded unit, and thus can be controlled. This application performs baseline sequential DCT-based JPEG decompression on photographic images

Features:

- Baseline ISO/IEC 10918-1 standard
- 8x8 two dimensional inverse DCT using fixed point
- Configurable Quantization tables
- 8 bit per pixel
- Supports color components in 4:4:4, 4:2:2 and 4:2:0 formats and black and white image

Block Diagram:

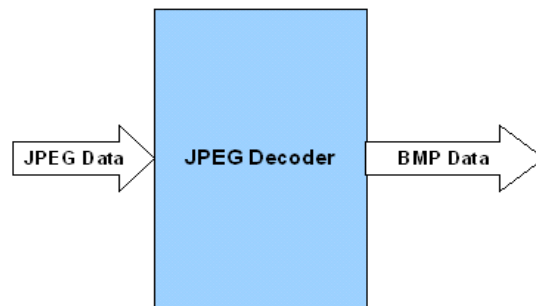


Figure 1: Block Diagram

Architectural Diagram:

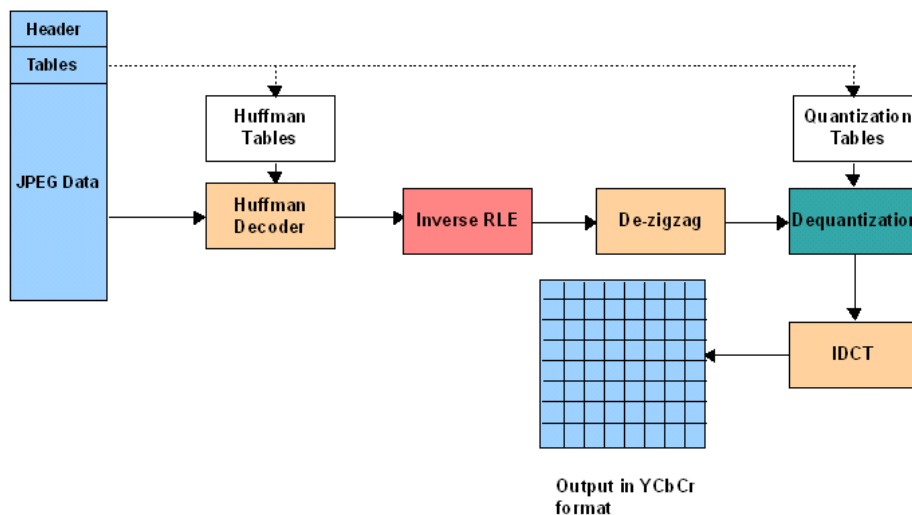


Figure 2: JPEG decoder Architecture Diagram

Description:

- The preceding module checks whether the `get_data` signal from the decoder is high or not.

If high, the the preceding module starts feeding data to the decoder, along with data_valid signal. When the last data is presented, the preceding module also gives the eoi_in signal high for a cycle.

- The preceding keeps checking for the get_data signal throughout. Whenever this signal goes low the preceding module stops sending data.
- At the output side, the signal DCT_final_out gives the output data. The signal final_valid_out

indicates when the output is valid.

- The signal final_soi_out is held high for a cycle when the first byte is outputted, and the signal final_eoi_out is held high for a cycle when the final byte is outputted.
- The mode signal is a constant output which shows whether the image being decompressed is a 4:4:4, 4:2:2, 4:2:0 colour image or a b/w image.

JPEG Decoder Core Parameter Table

JPEG_FILENAME	String	Useful for simulation only. Gives the name and location of the input bitmap file
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Signal definition table:

Signal	Direction	Description
datain[7:0]	IN	This is the data input to the module
datain_valid	IN	This signal indicates that data given to the module is valid.
eoi_in	IN	This signal is held HIGH for one cycle when the last data byte is given
clock	IN	This is the system clock
reset	IN	This is the system reset
DCT_final_out[7:0]	OUT	This is the output in YCbCr format
final_out_valid	OUT	This is the valid signal for the output
final_soi_out	OUT	This signal is held high for one cycle when the first output data arrives
final_eoi_out	OUT	This signal is held high for one cycle when the last output data arrives
final_YCbCr_out[1:0]	OUT	This signal indicates the kind of data block being outputted 01 – Y data block 10 – Cb data block 11 – Cr data block
image_height[15:0]	OUT	This output gives the image height
image_width[15:0]	OUT	This output gives the image width
get_data	OUT	This signal indicates to the preceding module whether the decoder is ready to accept data or not.
mode[2:0]	OUT	This gives the type of JPEG file that is decompressed. 001 – 4:4:4 colour image 010 – 4:2:2 colour image 011 – 4:2:0 colour image 100 – black and image image

Schematic Symbol:

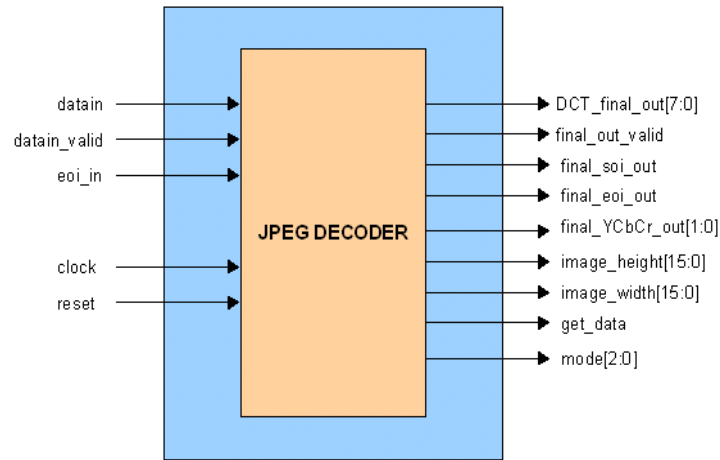


Figure 3: Schematic Symbol

Performance:

Device	Slice LUT Count	Slice Register Count	Frequency
Virtex-4 lx25 -10ff668	5577	2599	66 MHz
Virtex-5 lx50t -3ff1136	4234	2572	136 MHz

JPEG Decoder Frame Rate:

The following table shows possible frame rate with JPEG decoder running on Altera Stratix III or Xilinx Virtex-5 device at 120 MHz.

Image Type	Resolution		Possible Frame Rate Per Sec (At 120 MHz) at different YCbCr format		
	Width	Height	4:2:0	4:2:2	4:4:4
VGA	640	480	238	178	119
NTSC	720	480	211	158	105
PAL	720	576	176	132	88
HD	1280	720	79	59	39
HD	1920	1080	35	26	17

Verification:

The JPEG Decoder module has been verified with following approaches:

- Exhaustive Functional/Timing simulation.

Deliverables:

- Verilog RTL source code
- Test benches
- Synthesis and Simulation scripts.
- Detailed user documentation, including RTL source code documentation