

## Data sheet for I2S Core

### Functional Description:

I2S (Inter-IC Sound) is a serial link developed for digital audio. Digital audio systems have a lot of VLSI ICs which process the digital audio signals. These include A/D and D/A converters, Digital signal processors, Digital filters etc. I2S provides a standardized communication structure for communication between various digital signal

processing ICs.

### Features:

- Includes I2S transmitter and I2S receiver
- Supports configurable data width
- Supports configurable clock rate

### Block Diagram:

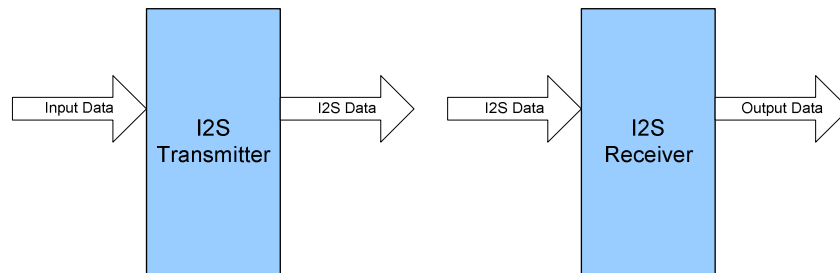


Figure 1: Block Diagram

### Architectural Diagram:

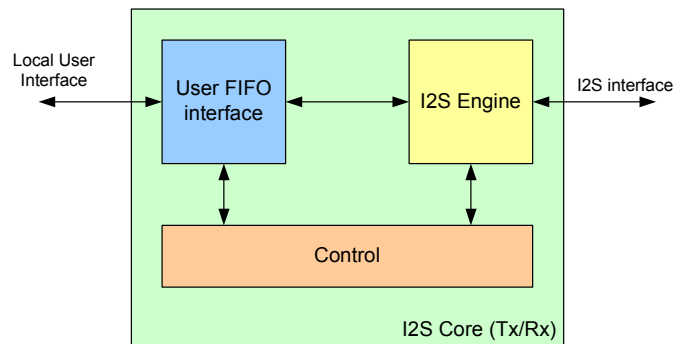


Figure 2: I2S Architecture Diagram

### Description:

1. Initially, the data is stored in FIFO in user logic domain
2. The I2S Transmitter Core checks this FIFO for availability of data.
3. Whenever data is available in the FIFO, the I2S Transmitter core reads this FIFO.
4. The FIFO data is assumed to be arranged as L+R channel samples. The FIFO width is DATA\_WIDTH and Left and Right channel data are stored alternatively.

5. This audio data is read from FIFO and serialized and sent out on I2S link.
6. The I2S stream is received from I2S link by I2S Receiver core.
7. The data is deserialized and written into FIFO in user logic domain. The Left and Right channel samples are written alternatively into the FIFO.
8. The user logic can monitor this FIFO and read out the audio data.

## I2S Parameter Table

This table describes the general I2S parameters:

<b>Parameter</b>	<b>Type</b>	<b>Description</b>
DATA_WIDTH	Integer	Data width of audio samples
ADDR_WIDTH	integer	Input clock to I2S Clock ratio

## Signal definition table:

### I2S Transmitter Core

<b>Signal</b>	<b>Direction</b>	<b>Description</b>
fifo_empty	IN	FIFO status signal indicating no data is available in the FIFO.
audio_data	IN	Input data port. This is the output data port of FIFO.
clk	IN	This I2S system is single clock system and all I/Os and internal I2S Engine is in synchronous with it.
rst_n	IN	This signal resets the system whenever it is asserted.
rd_req	OUT	Data request signal to FIFO.
if_clk	OUT	Clock to FIFO.
i2s_sck	OUT	I2S interface clock port The FIFO transactions between I2S Transmitter core and FIFO are done at this clock.
i2s_wd	OUT	I2S interface Word select port
i2s_sdo	OUT	I2S interface serial data port

### I2S Receiver Core

<b>Signal</b>	<b>Direction</b>	<b>Description</b>
fifo_full	IN	Real inputs. datain_Re is the port through which input will be fed. For N point input, it will take N cycles to feed the entire data.
clk	IN	This I2S system is single clock system and all I/Os and internal I2S Engine is in synchronous with it.
rst_n	IN	This signal resets the system whenever it is .
i2s_sck	IN	I2S interface clock port
i2s_wd	IN	I2S interface word select port
i2s_sdo	IN	I2S interface serial data port
audio_data	OUT	Audio data received on I2S link.
wr_req	OUT	FIFO write request signal
if_clk	OUT	Clock to external FIFO. The FIFO transactions between I2S Receiver core and FIFO are done at this clock.

**Schematic Symbol:**

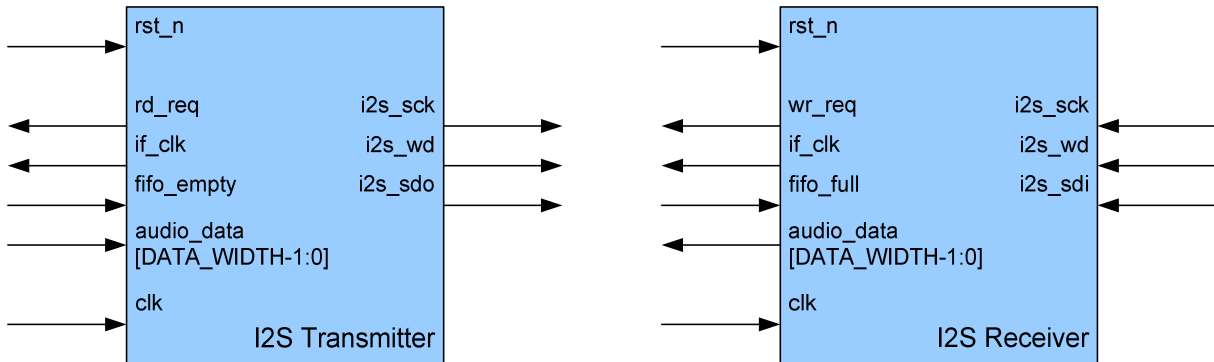


Figure 3: Schematic Symbol

**Verification:**

The I2S module has been verified with following approaches:

- Exhaustive Functional/Timing simulation.
- Interfacing with Open Cores I2S core

**Deliverables:**

- Verilog RTL source code
- Test benches
- Synthesis and Simulation scripts.
- Detailed user documentation, including RTL source code documentation