

## Data sheet for HDMI Transmitter Core

### Functional Description

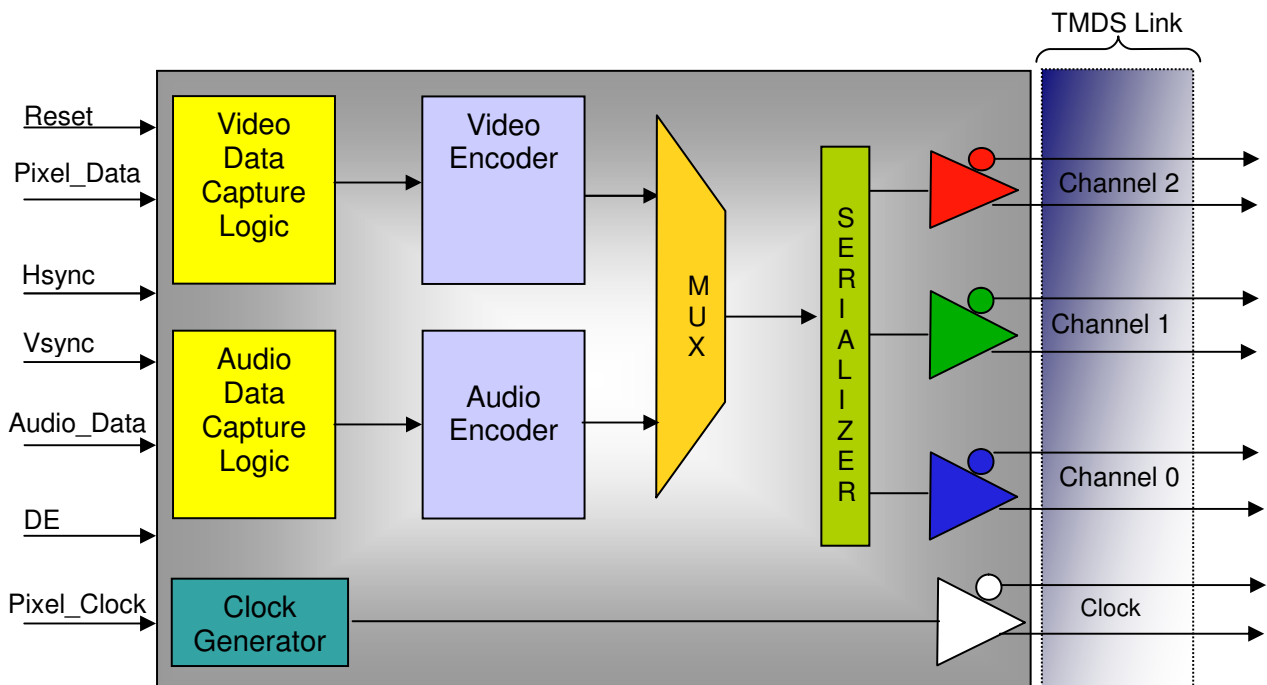
High-Definition Multimedia Interface (HDMI) is a digital video, audio and control interface standard which transmits uncompressed Video/Audio over serial link for the best quality. It accepts RGB (8-bit each) data, encodes it using transition minimized encoding technique (TMDS encoder) and transmits the encoded data over serial link. The TMDS encoder encodes each 8-bit pixel data into 10-bit DC-balanced. It also accepts 4-bit audio data (each channel) using Transition-Minimized Differential Signaling Error Reduction Coding-4 (TERC4) encodes it to 10-bit. The 10-bit codeword for both audio and video is serialized by the serializer and transmitted over three pair of serial data port. As audio/video data is digitally transmitted, it maximize visual/sound quality of digital devices such HDTV, flat panel LCD, computer monitors and digital projectors.

The high-definition multimedia interface (HDMI) specification is an industry standard adopted by many customer electronics manufacturers for high-speed digital connection to digital audio/video device. A HDMI connection consists of single TMDS serial link. A HDMI link consists of four pairs of wires (red, green, blue, and clock) to transmit 24 bits per pixel. The picture is transmitted line by line with blanking intervals between each line and each frame.

### Features:

- Supports 25-165M pixels/second
- Support resolutions from VGA to HDTV (640x480, 720x480p, 720x576p, 1280x720p, 1920x1080i)
- Interface support 24-bit RGB, 24-bit YCbCr (4:4:4) and 12-bit YCbCr (4:2:2) inputs.

### Block Diagram



### HDMI Parameter Table:

<b>Parameter</b>	<b>Description</b>
h_res	Horizontal resolution of active video period.
v_res	Vertical resolution of active video period.
h_front	Horizontal front porch period
h_sync	Horizontal sync period
h_back	Horizontal back porch period
v_front	Vertical front porch period
v_sync	Vertical sync period
v_back	Vertical back porch period

**Signal Definition Table:**

<b>Signal Name</b>	<b>Width</b>	<b>Direction</b>	<b>Description</b>
reset	1	Input	System Reset
pixel_clock	1	Input	System Clock. All registers are synchronized to rising edge of this signal. (27MHz or 74.25MHz depending on required resolution)
pixel_data	24	Input	24-bit RGB data to the encoder.
audio_data	12	Input	12-bit audio data.
hsync	1	Input/Core	This control signal is sent on channel0. This signal may be provided by user as input to the core or it can be generated internally in HDMI core.
vsync	1	Input/Core	This control signal is sent on channel0. This signal may be user input to the core or it can be generated internally in HDMI core.
DE	1	Input/Core	This control signal is used to indicate active display period. This signal may be user input to the core or it can be generated internally in HDMI core.
Channel 0	2	Output	TMDS (Differential) link for transmitting blue color serially.
Channel 1	2	Output	TMDS (Differential) link for transmitting green color serially.
Channel 2	2	Output	TMDS (Differential) link for transmitting Red color serially.
clock	2	Output	This is differential pixel clock signal send on clock channel.

**Verification:**

The HDMI transmitter core module has been verified with following approaches:

- Exhaustive Functional/Timing simulation.
- Tested with HDMI TV with 480p, 576p, 720p and 1080i prototyped on Xilinx FPGA

**Deliverables:**

- Verilog RTL source code
- Test benches
- Synthesis and Simulation scripts.
- Detailed user documentation, including RTL source code documentation