

## Datasheet for I2C EEPROM Controller

### Functional Description:

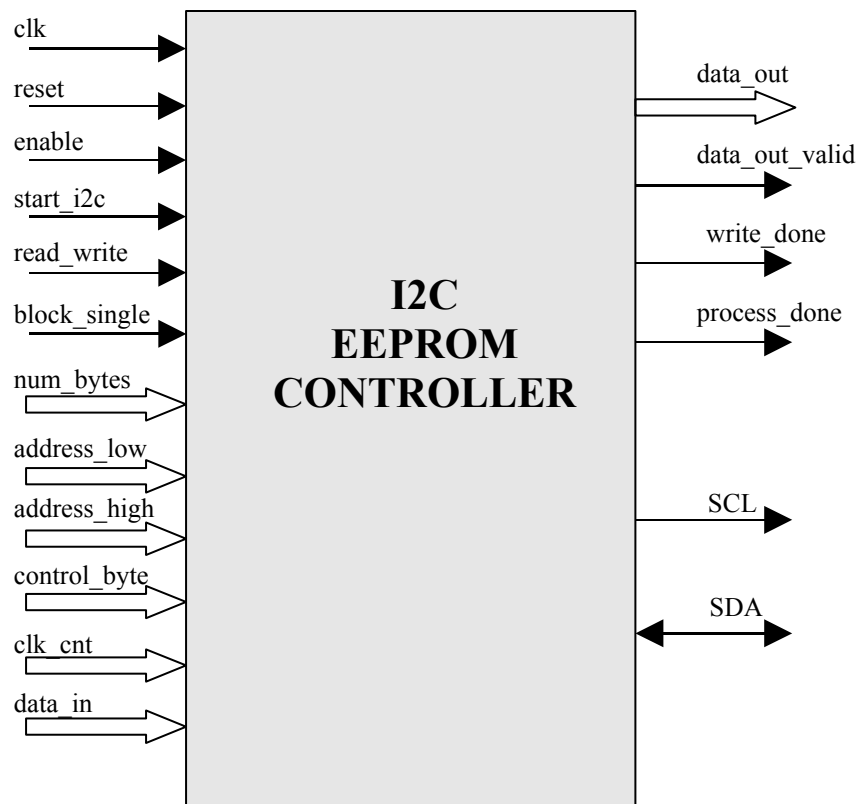
I2C is a two wire, bidirectional serial bus that provides effective data communication between two devices. I2c bus supports many devices, each device is recognized by a unique address—whether its a micro-controller, LCD Driver, memory or keyboard interface and can operate as transmitter or receiver based on the functioning of the device.

The controller designed controls the EEPROM device through I2C protocol. The I2C Controller here acts as a master device and controls EEPROM which acts as a slave.

### Features:

- Full duplex serial data transfer
- MSB data transfer first
- Single byte and Busrt Data write and read operation supported
- Supports 7 Bit Addressing
- Several EEPROM slaves can be connected to the I2C Controller based on the input control word.
- Programmable Serial clock.
- Standard Verilog Soft core
- Fully Synthesizable

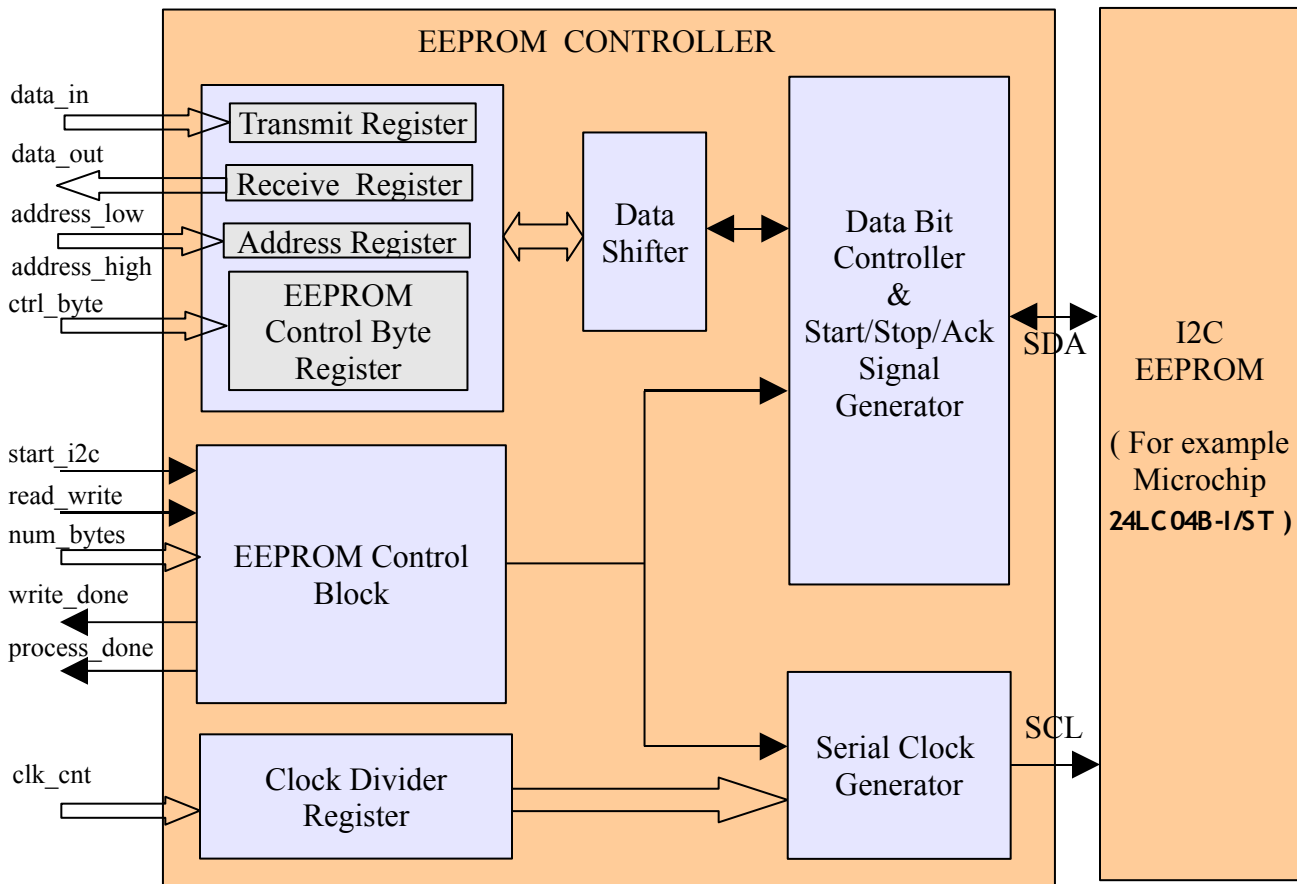
### Symbol:



## Pin Descriptions:

Pin	Type	Width	Description
clk	input	1	Input Clock
reset	input	1	Active High reset input
enable	input	1	Active High Enable pin
start_i2c	input	1	One cycle active high input which starts I2C operation
read_write	input	1	Read/write operation flag
block_single	input	1	Flag which indicates burst or single operation
num_bytes	input	8	Number of bytes to read or write in burst operation
address_low	input	8	Lower 8 bit Address of EEPROM
address_high	input	8	Higher 8 bit Address of EEPROM
control_byte	input	7	Control Byte for EEPROM
clk_cnt	input	8	Counter for Clock Divider
data_in	input	8	8 bit data to be written to EEPROM
data_out	output	8	8 bit data read from EEPROM
data_out_valid	output	1	Data valid signal for data_out
write_done	output	1	Flag write done signal after every byte write in Burst write Operation
process_done	output	1	I2C Operation complete flag
SCL	output	1	Serial Clock Line of I2C
SDA	inout	1	Serial Data Line of I2C

**Block Diagram:**



**Description:**

**Register's Set and Shifter:**

The register set consists of Transmit/Receive Register, Address Register and EEPROM Control Byte Register. The Address Register stores the address of EEPROM into which the data is to be read or written. 7 bit EEPROM Control byte register stores the Control Byte of the EEPROM slave. Transmit and Receive Registers are used for storing the data in and out from the I2C EEPROM.

Data Shifter Block shifts the data bit by bit into the Bit Controller Block.

**EEPROM Control Block:**

This Block controls the EEPROM operation. Enabling start\_i2c for one cycle initiates the I2C transfer. The read\_write flag tells the Controller whether to write or read the data from EEPROM. Once the transfer is initiated, the Controller reads the data form the data\_in port and writes into EEPROM or reads the data from EEPROM and output it at data\_out port based on the operation selected.

For Burst read/write operation, num\_bytes input indicates the number of data bytes to be read or written into EEPROM. For Burst write Operation, when the single byte is written, write\_done signal is set for one cycle after which the user has to append next byte into the data\_in port. Once the operation is complete, process\_done signal is set.

**Data Bit Controller and I2C Signal Generator:**

This Block generates I2C Signals based on the control input from EEPROM Control Block. This block also generates Start, Stop, Acknowledge and Repeated start signals.

**Serial Clock Generator:**

The I2C Serial Clock is frequency is generated based on the "clk\_cnt" input based on the formula

$$I2C_{SCLK} \text{ Frequency} = \text{System Clock Frequency} / 8 * (\text{clk\_cnt} + 1)$$

Clock Divider Register stores the value of the input clk\_cnt.

**Performance:**

Device	Slice Count	Frequency
Spartan-3A (xc3s700a-4fg484)	207	150 MHz
Virtex-4 (xc4vlx25-ff668)	212	330 MHz

**Verification:**

The I2C controller module has been verified with following approaches:

- Exhaustive Functional/Timing simulation
- Prototyped on Xilinx Virtex-4 Board and tested on I2C EEPROM (Microchip Technology 24LC04B-I/ST)

**Deliverables:**

- Verilog RTL source code
- Test benches
- Synthesis and Simulation scripts
- Detailed user documentation, including RTL source code documentation