

## Data sheet for Dilation/Erosion Core

### Introduction:

Morphology deals with shapes of images in Image processing. The value of the each output pixel is based on a comparison of the corresponding pixel in the input image with its neighborhood pixels. The size and shape of the structural element determines the morphological operation to be done on a particular image. Morphological operations are usually applied to the processing of binary and greyscale images. Fundamental operations are Dilation and Erosion. From these two basic operations, other operations like opening and closing of an image are developed. The principle of Dilation operation is the the value of the output pixel is the maximum value of all the pixels in the input pixels neighborhood. In Erosion, the value of the output pixel is the minimum value of all pixels in their input pixel's neighborhood. Structuring element consists of 1's and 0's and the size is much smaller than input image. The center of the structuring element identifies the pixel being processed.

### Functional Description:

Structuring element is chosen properly according to the requirements. This structuring element is moved over the entire input image, with center of structuring element is coincided with the pixel of interest and the output pixel corresponds to this pixel being processed is either maximum (Dilation) or minimum (Erosion) of all pixels in the neighborhood pixels. This operation is done for all input image pixels and thus output dilated/eroded image is found. The size and shape of the structuring element decides the output image. By properly choosing this element, one could get the desired morphological operation on the input image.

### Features:

- High speed morphological operation algorithm.
- Configurable dilation and Erosion functionality
- Compatible with all images resolutions
- Synchronous design
- Configurable input image size and structuring element size
- Available for Xilinx FPGA
- Compatible, flexible and easy integration with other modules

### Block Diagram:

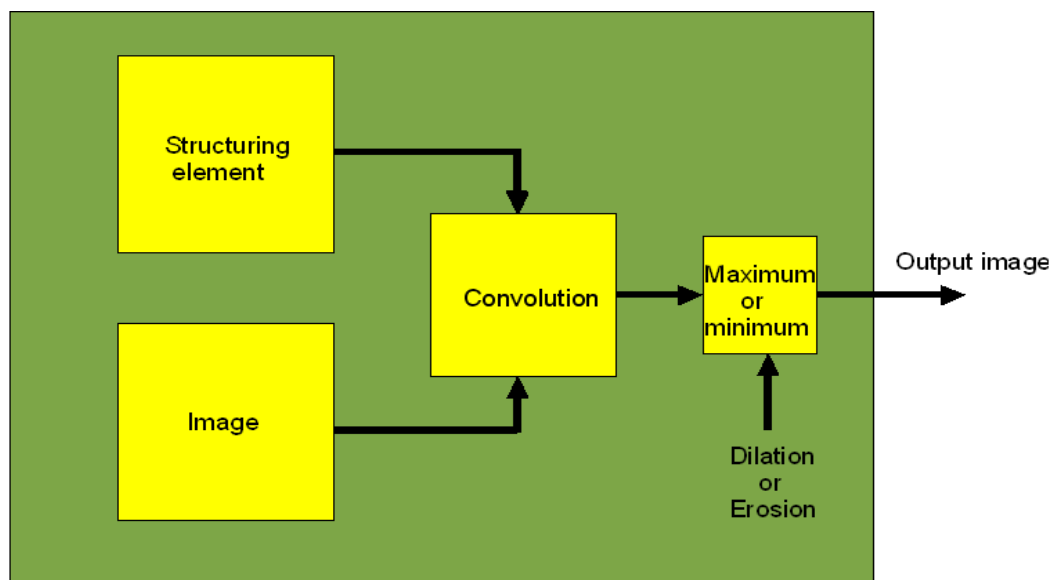


Figure 1: Dilation/Erosion Block Diagram

**Architecture Diagram:**

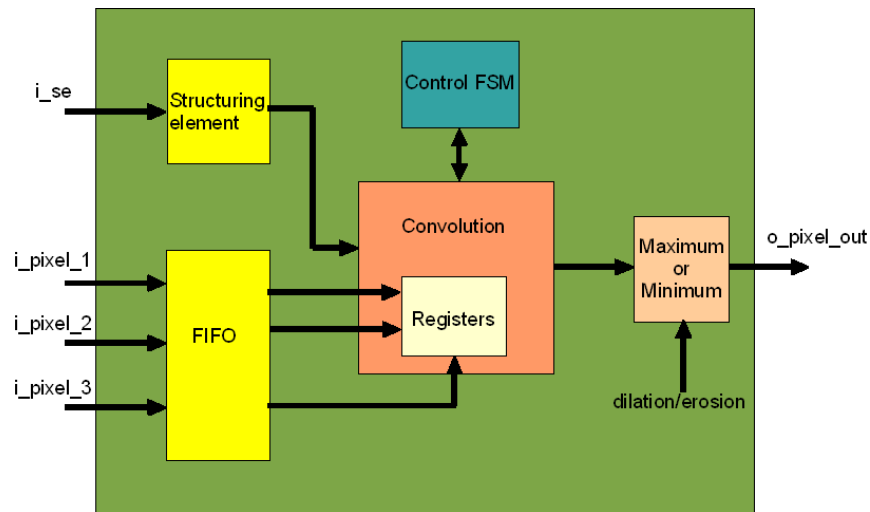


Figure 2: Dilation/Erosion core Architecture Diagram.

**Description:**

- Figure.1 shows the block diagram of the Dilation/Erosion IP core.
- It consists of input image, structuring element, convolution block and maximum/minimum blocks.
- The desired structuring element with appropriate size and shape is convolved with input image by convolution block. Then maximum/minimum (Dilation/Erosion) of neighborhood pixels is found by Maximum/Minimum block.
- Fig.2. represents the architectural diagram of the Dilation/Erosion core.
- Input pixels are written into FIFO. Structuring elements which are coming from input port **i\_se** are stored in internal memory.
- The FIFO data is read and stored in internal memory and the depth of the memory depends

- upon the size of the structuring element.
- Then structuring element is convolved with these input image pixels and the output pixel which is either maximum(Dilation) or minimum(Erosion) is done.
- Table. 1 represents the all parameters used in the Dilation/Erosion IP core. The parameter **OPERATION** (shown in Table.1) determines which operation (Dilation or Erosion) has to be done.
- Fig. 3 represents the schematic symbol of the Dilation/Erosion IP core. It shows all input and output ports with their port width.
- Table. 2 describe all input and output ports briefly about their function, type (IN/OUT) of port and width of port.
- Table. 3 indicate the performance numbers of the Dilation/Erosion core and its slice count.

**Dilation/Erosion Parameter Table:**

<b>Parameter</b>	<b>Type</b>	<b>Description</b>
WL	Integer	Represents width of the each data symbol.
OPERATION	Integer	Represents what operation has to be done on the input image data. '1' means " <b>Dilation</b> " '0', means " <b>Erosion</b> "

Table 1: Dilation/Erosion Parameter table.

**Schematic Symbol:**

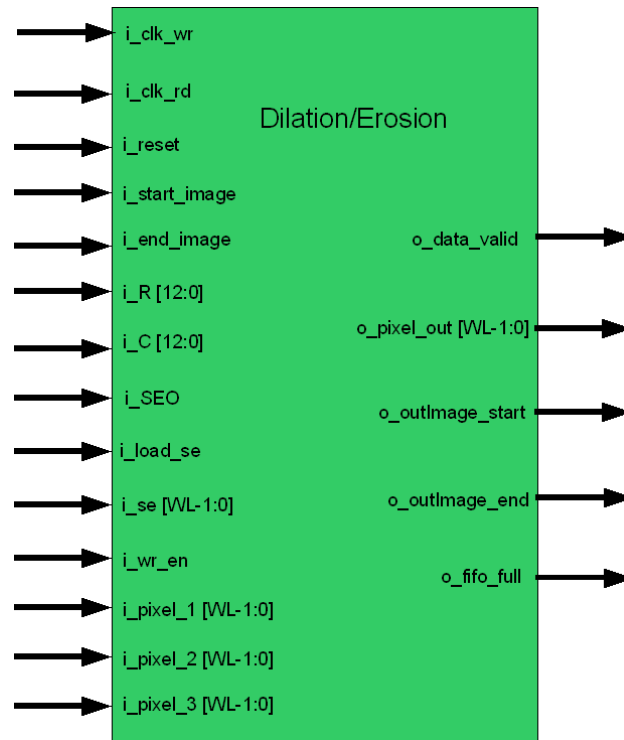


Figure 3: Dilation/Erosion Schematic Symbol

**Signal definition table:**

<b>Signal</b>	<b>Direction</b>	<b>Data width</b>	<b>Description</b>
i_clk_rd	IN	1	This clock is used to synchronize entire logic from FIFO output onwards.
i_clk_wr	IN	1	FIFO writing is done with respect to this clock.
i_reset	IN	1	This signal resets the system whenever it is enabled and all counters, registers are set to initial value to hold and state machines are set to starting state.
i_start_image	IN	1	This is single bit input signal which is enabled when first pixel of a new image frame is presented at the input port. Otherwise disabled.
i_end_image	IN	1	This is single bit input signal which is enabled when last pixel of an current image frame appears at input port. Otherwise disabled.
i_R	IN	13	This is 13 bit input port which specifies the number of rows of the image
i_C	IN	13	This is 13 bit input port which specifies the number of columns of the image

<b>Signal</b>	<b>Direction</b>	<b>Data width</b>	<b>Description</b>
i_SEO	IN	WL	This is WL bit width input port through which size of the structural element is given to the Dilation/Erosion core.
i_load_se	IN	1	This is single bit input port which is enabled when structural element data comes to the input port. And get disabled when there is no data.
i_se	IN	WL	This is <b>WL</b> bit input port through which structural element data will be loaded.
i_wr_en	IN	1	This is single bit input port when enabled, pixel data started writing into FIFO. And when complete image is fed, this signal gets disabled.
i_pixel_1 i_pixel_2 i_pixel_3	IN	WL	This is WL bit width input port through which three pixels of gray scale image are sent to core.
o_data_valid	OUT	1	Asserted when data is valid on port o_pixel_out
o_pixel_out	OUT	WL	This is WL bit width output port through which Dilation/Erosion core outputs dilated/Eroded pixel data.
o_outImage_start	OUT	1	This signal is enabled when first pixel of resultant dilated/eroded image comes out of the output port o_pixel_out.
o_outImage_end	OUT	1	This signal is enabled when last pixel of resultant dilated/eroded image comes out of the output port o_pixel_out
o_fifo_full	OUT	3	This is 3 bit width output port which is enabled when FIFO is full of data.

Table 2: Dilation/Erosion signal definition table

#### Performance:

<b>Device</b>	<b>Slice Count</b>	<b>Frequency (MHz)</b>
Virtex-4	412	268
Virtex-5	476	310

Table 3: Dilation/Erosion Core Performance table

#### Verification:

The Dilation/Erosion core module has been verified with following approaches:

- Exhaustive Functional/Timing simulation
- Results compared with MATLAB functions and C source code functionality.

The Dilation/Erosion core has been tested for gray images. The following industry resolution images are tested on Dilation/Erosion core.

- 256x256 resolution

- VGA resolution images (640 X 480).
- HD resolution images (1920 X 1080)

#### Deliverables:

- Verilog RTL source code
- The IP core test environment developed in verilog HDL (test benches)
- Synthesis and Simulation scripts
- Detailed user documentation, including RTL source code documentation.

**Applications:**

The following are the applications of Dilation/Erosion in Image processing.

- Noise removal and smoothing of images: Opening followed by closing removes structures and holes smaller than the structuring elements.
  - Image boundary detection
  - Region filling.
  - Bridging gaps in images.
  - Extraction of connected components in images.
- Thinning of an image.
  - Thickening of an image.
  - Pruning of an image.
  - Contrast enhancement of images.
  - Skeletonization of the image: To reduce all objects in an image to lines, without changing the structure of the image.
  - Morphological gradient.
  - Top-hat transformation.
  - Textural segmentation.
  - Granulometry.