

## Data sheet for DVI Transmitter Core

### Functional Description

Digital Video Interface (DVI) is a video interface standard which transmits uncompressed Video over serial link. It accepts RGB (8-bit each) data, encodes it using transition minimized encoding technique (TMDS encoder) and transmits the encoded data over serial link. The TMDS encoder encodes each 8-bit pixel data into 10-bit DC-balanced and then the 10-bit codeword is transmitted serially. As video data is digitally transmitted, it maximize visual quality of digital display devices such flat panel LCD, computer monitors and digital projectors.

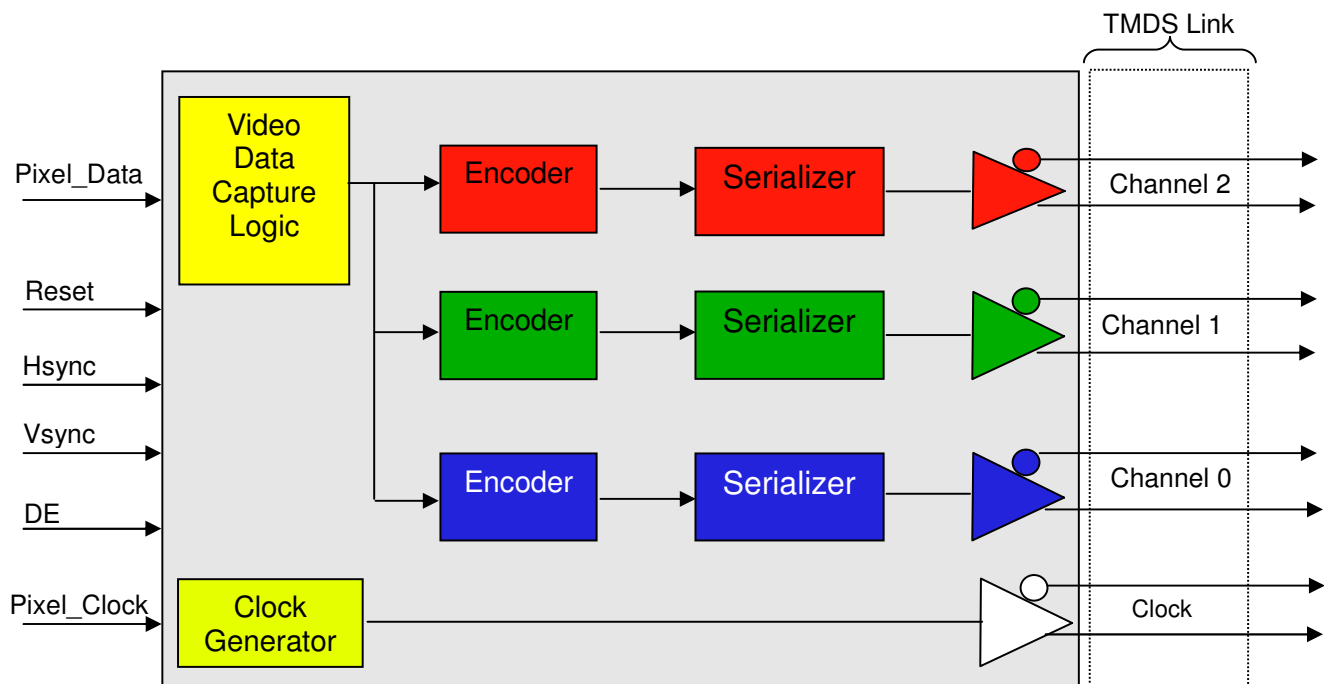
The digital visual interface (DVI) specification is an industry standard developed by the digital display working group (DDWG) for high-speed digital connection to digital displays and has been

adopted by industry- leading PC and consumer electronics manufacturers. A DVI connection consists of single or dual TMDS serial link. A single DVI link consists of four twisted pairs of wires (red, green, blue, and clock) to transmit 24 bits per pixel. The picture is transmitted line by line with blanking intervals between each line and each frame. No compression is used and there is no support for only transmitting changed parts of the image. This means that the whole frame is constantly re-transmitted.

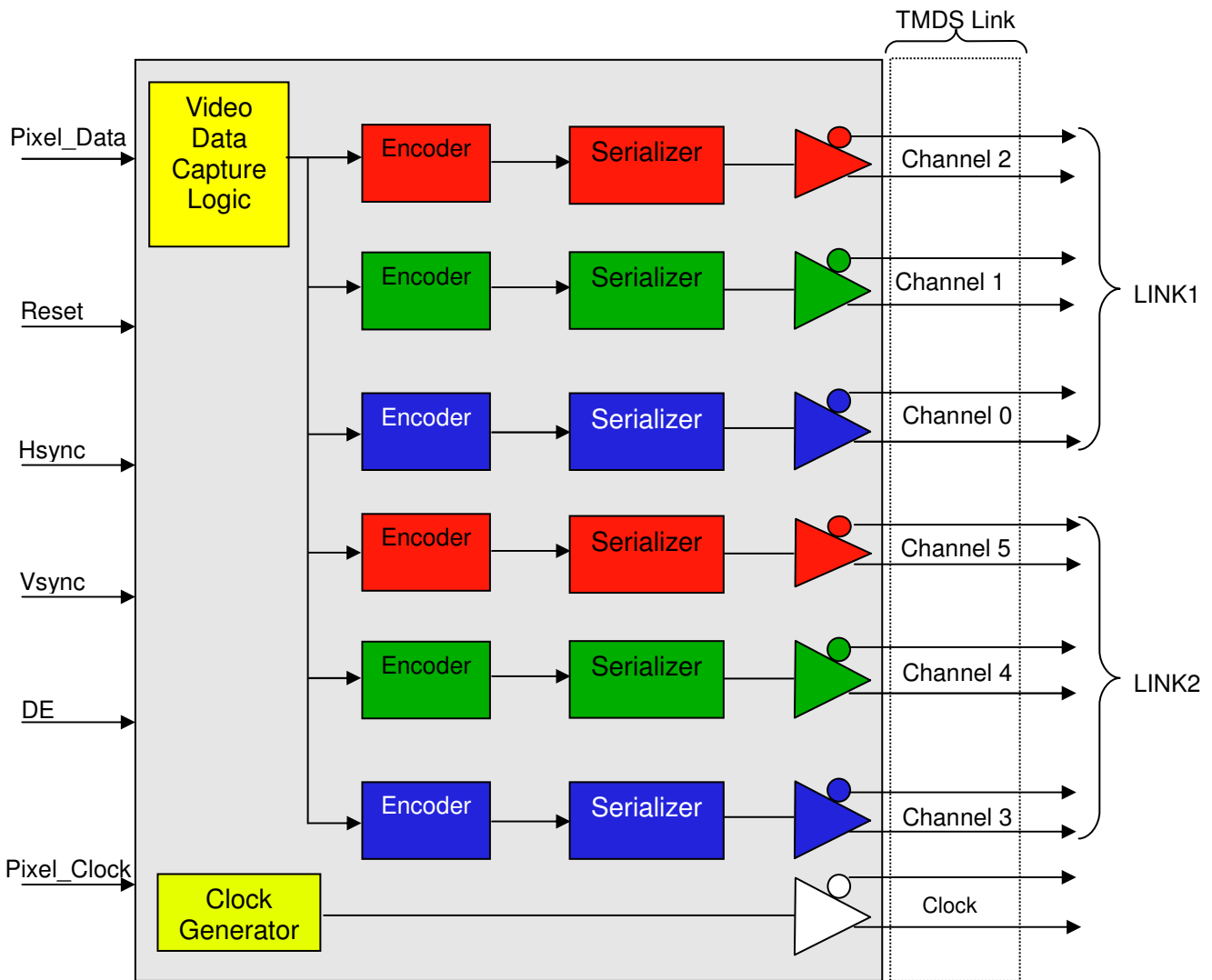
### Features:

- Supports 25-165M pixels/second
- Support resolutions from VGA to UXGA
- Interface support 24-bit RGB input
- Support single link and dual link channel

### Single Link Block Diagram



**Dual Link Block Diagram**



**Parameter Table:**

<b>Parameter</b>	<b>Description</b>
Dual_Link	Configure DVI core for Single or Dual link.
h_res	Horizontal resolution of active video period.
v_res	Vertical resolution of active video period.
h_front	Horizontal front porch period
h_sync	Horizontal sync period
h_back	Horizontal back porch period

v_front	Vertical front porch period
v_sync	Vertical sync period
v_back	Vertical back porch period

**Signal definition table:**

<b>Signal Name</b>	<b>Width</b>	<b>Direction</b>	<b>Description</b>
reset	1	Input	System Reset
pixel_clock	1	Input	System Clock. All registers are synchronized to rising edge of this signal.
pixel_data	24	Input	24-bit (for single link) and 48-bit (for dual link) RGB data to the encoder.
hsync	1	Input	This control signal is sent on channel0. This signal may be provided by user as input to the core or it can be generated internally in DVI core.
vsync	1	Input	This control signal is sent on channel0. This signal may be user input to the core or it can be generated internally in DVI core.
DE	1	Input	This control signal is used to indicate active display period. This signal may be user input to the core or it can be generated internally in DVI core.
Channel 0	2	Output	TMDS (Differential) link for transmitting blue color serially.
Channel 1	2	Output	TMDS (Differential) link for transmitting green color serially.
Channel 2	2	Output	TMDS (Differential) link for transmitting Red color serially.
Channel 3	2	Output	TMDS (Differential) link for transmitting blue color serially. This link is active for dual link DVI mode.
Channel 4	2	Output	TMDS (Differential) link for transmitting green color serially. This link is active for dual link DVI mode.
Channel 5	2	Output	TMDS (Differential) link for transmitting Red color serially. This link is active for dual link DVI mode.
clock	2	Output	This is differential pixel clock signal send on clock channel.

**Performance:**

<b>Device</b>	<b>Slice Count</b>	<b>LUT Count</b>	<b>Frequency</b>	<b>Resolution</b>
Spartan-3A (xc3s700A)	255	476	123.22 MHz	640x480, 800x600

**Verification:**

The DVI transmitter core module has been verified with following approaches:

- Exhaustive Functional/Timing simulation.
- Tested with DVI monitors and projectors
- Verified both Single and Dual links

**Deliverables:**

- Verilog RTL source code
- Test benches
- Synthesis and Simulation scripts.
- Detailed user documentation