

## Data sheet for BT656/601 Interface

### Functional Description

The BT656/601 interface is a parallel interface which receives 8-bits of multiplexed YCbCr data and uses a 27MHz clock. This block can support both ITU-R BT601 format as well as ITU-R BT656 format. The only difference between the two modes is that in BT601 mode, the timing information is available through the input sync pulses and in BT656 mode the timing information is embedded in the data stream.

The incoming data is in multiplexed YCbCr 4:2:2 format. The BTIF demultiplexes the Y0, Cb0, Y1 and Cr0 data from the data stream and outputs them on separate lines at the appropriate time. The output from BTIF is used by the subsequent

stages of Video processing.

In addition this block also generates color bars internally during operation in test mode.

The BTIF is an essential block in all digital video processing systems.

### Features:

- Supports BT601 and BT656 formats
- Supports NTSC(M), PAL(B,D,G,H,I), PAL (M) and PAL(N) and SECAM video formats
- Color Bar mode support
- Ancillary data (WSS and CGMS) extraction
- Internal HSYNC and VSYNC Generation in BT656 and color bar modes

### Block Diagram:

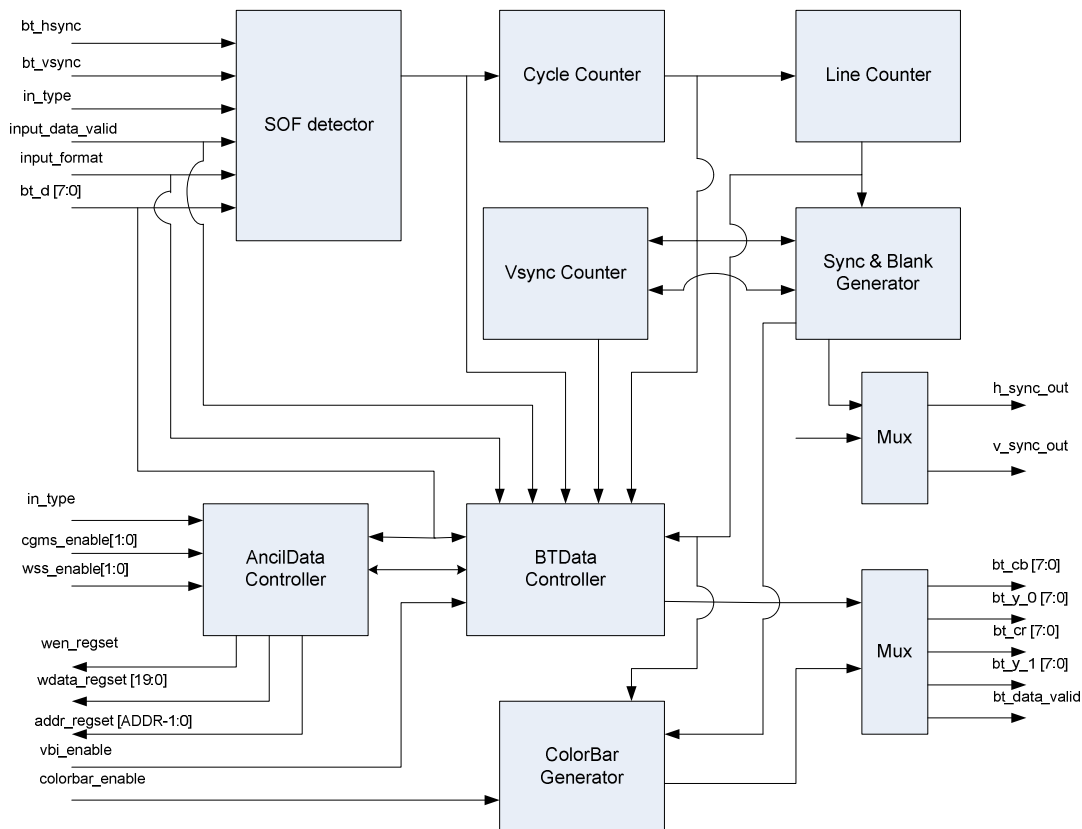


Figure 1: BT656 Block Diagram

### Description:

The BTIF block is enabled using either one of two signals namely *input\_data\_valid* or *colorbar\_enable*. When *input\_data\_valid* is set, it implies that BTIF will be operating in either BT656 or BT601 mode depending on the *input\_format* signal value. When *colorbar\_enable* is set, the incoming data will be ignored and internally generated color bar pattern will be output. *colorbar\_enable* is usually set when one wants to operate the system in test mode.

Following is a brief description of the different blocks in BTIF.

**SOFdetector** : The SOFdetector detects the Start of Frame condition (using HSYNC and VSYNC in case of BT601 mode and using embedded SOF condition embedded in the data stream in case of 656 mode). In normal mode of operation, the rest of the blocks are enabled by the output of this block.

**Cycle Counter** : The cycle counter maintains a count of the number of bytes of data for each line of video. Once a line is complete, this counter is restarted.

**Line Counter** : This block keeps track of the line number that is currently being processed. Once a complete frame is completed this counter is restarted

**Sync Counter** : This block is a counter which keeps track of the number of cycles for which VSYNC should be maintained low.

**Sync and Blank Generator**: This block

generates the sync pulses internally and these internally generated sync pulses are output when operating in BT656 mode. Also it generates blanking pulses for internal use

**BTdata\_Controller** : This block is enabled in normal mode operation. During the active video portion, this block assigns the active video data to the respective output lines. A valid signal is generated every 4 clocks. When valid is high, we have 2 pixels of data output on the 4 output lines *bt\_cb*, *bt\_y\_0*, *bt\_cr*, *bt\_y\_1*. In case any ancillary data is present in the stream, This block enables the **Ancildata\_ctrl** block.

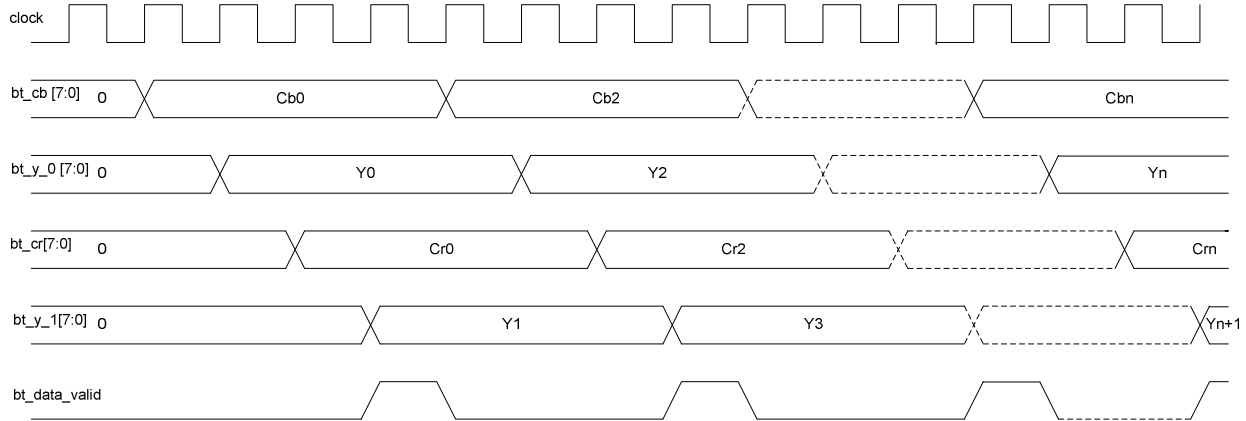
**Ancildata\_ctrl** : This block extracts the VBI data present in the data stream and generates the appropriate signals for writing the ancillary data to the appropriate VBI register. Currently WSS and CGMS VBI data extraction is supported.

**ColorBar Generator** : This block is enabled in test mode. It generates a known standard colorbar pattern (100% colorbars for PAL/NTSC/SECAM) in place of active video portion.

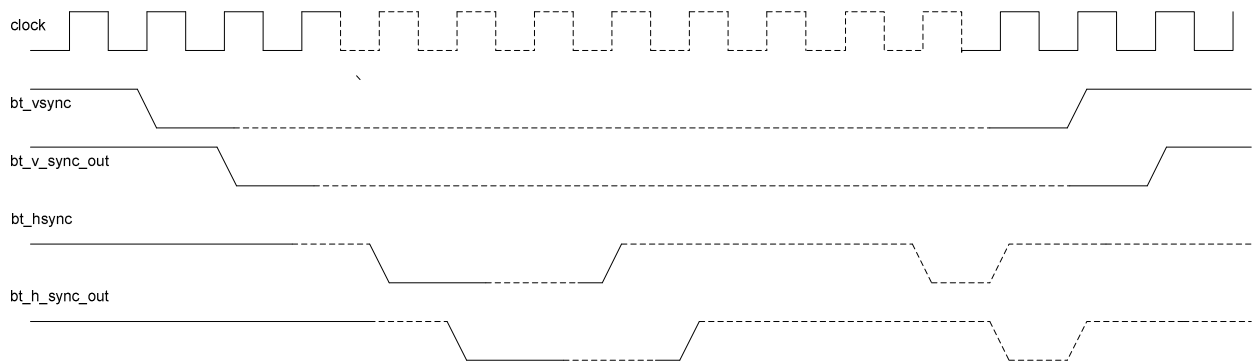
**Operational Frequency** : The entire system operates at a frequency of 27 MHz which is as per the ITU-R BT601 standard

**Input Format** : The input should be in compliance with the ITU-R BT601 and ITU-R BT656 standards.

### Timing Diagrams:



*Figure 2: Timing diagram for output data*



*Figure 3 : Relation between the input and output sync pulses*

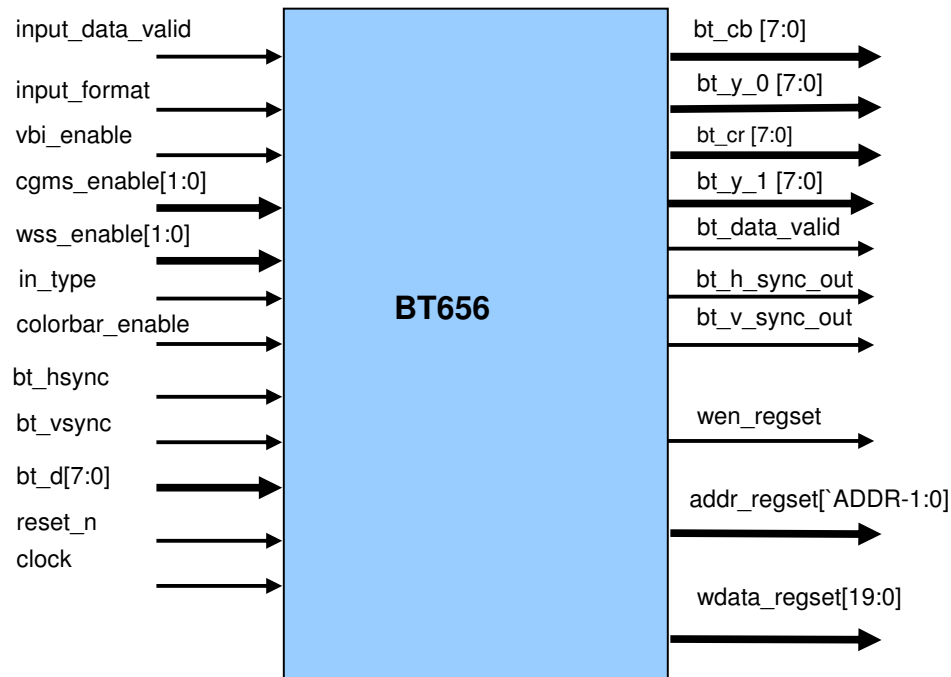
**Signal definition table:**

<b>Signal</b>	<b>Direction</b>	<b>Description</b>
input_data_valid	IN	Enable the BTIF in normal mode, accept the data from external video source
input_format	IN	1'b0 – BT601 mode 1'b1 – BT656 mode
clock	IN	The BTIF system is a single clock system and all I/Os and internal blocks are synchronous with it.
vbi_enable	IN	1'b1 : Enable extraction of ancillary data from data stream 1'b0 : Disable VBI extraction

<b>Signal</b>	<b>Direction</b>	<b>Description</b>
cgms_enable	IN	Valid only for NTSC , PAL (M) modes 2'b00 : Disable CGMS on both fields (default value for this signal in PAL 2'b01 : Enable CGMS data extractions on ODD field 2'b10 : Enable CGMS data extraction on EVEN field 2'b11 : Enable CGMS data extraction on both fields
wss_enable	IN	Valid only for PAL (B,D,G,H,I ,N) modes 2'b00 : Disable WSS on both fields (default value for this signal in NTSC 2'b01 : Enable WSS data extractions on ODD field 2'b10 : Enable WSS data extraction on EVEN field 2'b11 : Enable WSS data extraction on both fields usually WSS is enabled on only odd field
reset_n	IN	This signal resets the system whenever it is disabled and all counters, registers are sets to starting point.
in_type	IN	This signal indicates whether the input data is in NTSC /PAL format 1'b0 : NTSC(M), PAL(M) formats 1'b1 : PAL (B,D,G,H,I,N) formats
colorbar_enable	IN	Enables the colorbar (Test mode) operation. The incoming data stream and sync pulses are ignored
bt_hsync	IN	This port represents the Hsync pulse used during BT601 mode of operation
bt_vsync	IN	This port represents the Vsync pulse used during BT601 mode of operation
bt_d	IN	This signal is the 8-bit multiplexed YCbCr data stream. In BT656 mode, it also contains the EAV and SAV sequences as well as ancillary data
bt_h_sync_out	OUT	The hsync pulse output from BTIF. It could be either the incoming hsync pulse (in BT601 mode) or the internally generated hsync pulse(in BT656 or color bar mode)
bt_v_sync_out	OUT	The hvync pulse output from BTIF. It could be either the incoming vsync pulse (in BT601 mode) or the internally generated vsync pulse(in BT656 or color bar mode)
bt_cb	OUT	This port outputs the Cb data corresponding to a pixel . This is the output of a mux which selects between the data from data stream and that from the color bar generator
bt_y_0	OUT	This port outputs the Y0 data corresponding to the odd numbered pixel . This is the output of a mux which selects between the data from data stream and that from the color bar generator
bt_cr	OUT	This port outputs the Cr data corresponding to the a pixel . This is the output of a mux which selects between the data from data stream and that from the color bar generator
bt_y_1	OUT	This port outputs the Y1 data corresponding to the even numbered pixel . This is the output of a mux which selects between the data from data stream and that from the color bar generator

<b>Signal</b>	<b>Direction</b>	<b>Description</b>
bt_data_valid	OUT	The data valid port which indicates that the output data on the four data lines is valid. It goes high for one clock along with bt_y_1 signal
wen_regset	OUT	This port is the write enable for a register which stores ancillary data
addr_regset	OUT	This port is the address of the register to which the extracted ancillary data has to be written
wdata_regset	OUT	This port is the actual ancillary data to be written into the address specified by addr_regset

**Schematic Symbol**



**Performance:**

<b>Device</b>	<b>Slice Count</b>	<b>Frequency</b>
Virtex-4	425	90.29 MHz

**Verification:**

The BTIF module has been verified with following approaches:

- Reading real video data from a file.
- Data generated through behavioral models for the BT601 and BT656 drivers.
- Was integrated with other Video processing blocks and prototyped on ML-401 board for PAL

and NTSC data

**Deliverables:**

- Verilog RTL source code
- Test benches
- Behavioral models of the BT601 and BT656 drivers