

## Data sheet for BCH Encoder Core

### Introduction:

BCH codes are mainly used in communication systems requiring Forward Error Correction (FEC) as an error detector and correctors where data transmitted through communication channel is viable to errors and erasures. This can be targeted to both FPGA and ASIC technologies.

During encoding redundant data called parity symbols are appended to data symbols to detect and correct errors in the data during decoding. Usually these errors are mainly due to channel noise. The error correcting capability of depends upon number of parity data appended to actual data block.

The BCH encoder receives K symbol code word and appends with 2T symbols and then form N symbol code word. As a result BCH decoder can detect and correct up to T possible symbol errors or up to 2T symbol erasure symbol errors, where T is  $(N-K)/2$ . When number of errors presented in code word exceeds T, then decode failure occurs.

### Functional Description:

The encoders of BCH are conventionally implemented by a linear feedback shift register

(LFSR) architecture. Depending upon the N and K values, respective generator polynomial will be computed. Message input to encoder polynomial is shifted left by N-K positions and in that first N-K positions, parity symbols are computed and placed.

This parity polynomial is the mod of  $M(x) X^{(N-K)}$  and  $g(x)$ . Where,  $M(x)$  is the message polynomial and  $g(x)$  is the generator polynomial. All operations like multiplication and additions are done with respect to Galois field.

### Features:

- High speed BCH encoding algorithm.
- Fully compliant with standard such as DVB-s2 and DVB-S standards.
- Compatible with all code and data lengths.
- Synchronous design.
- Provision to change code rates dynamically.
- Available for Xilinx FPGA and ASIC implementation.
- Core can be configured for any value of code and data lengths N and K.
- Area and power optimized implementation
- Compatible, flexible and easy integration with other modules.

### Block Diagram:

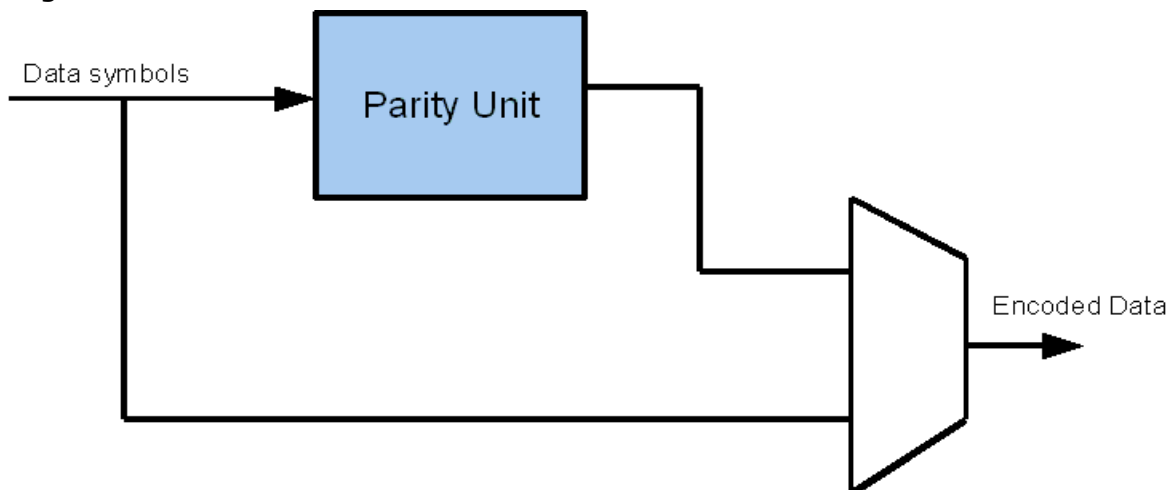


Figure 1: BCH Encoder Block Diagram.

**IP Parameters:**

This table describes the general BCH Encoder parameters:

<b>Parameter</b>	<b>Type</b>	<b>Description</b>
WL	Integer	Represents width of the each data symbol.

Table 1: BCH Encoder Parameter table.

**Schematic Symbol:**

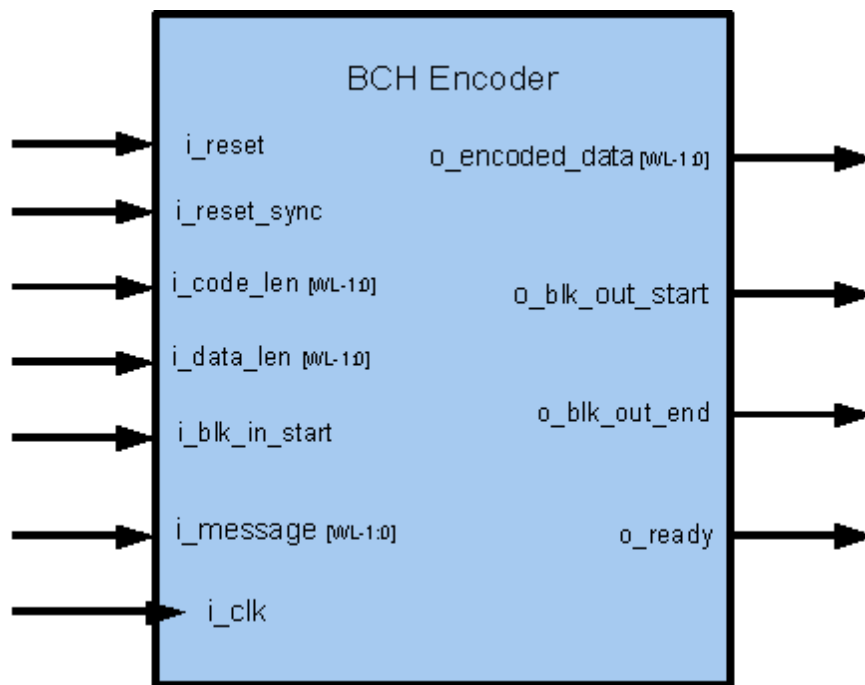


Figure 2: BCH Encoder Schematic Diagram

**Signal Definition:**

<b>Signal</b>	<b>Direction</b>	<b>Data width</b>	<b>Description</b>
i_clk	IN	1	This BCH Encoder is single clock system and all I/Os and internal encoder processor is in synchronous with it.
i_reset	IN	1	This signal resets the system whenever it is enabled and all counters, registers are sets to starting point.
i_reset_sync	IN	1	This is synchronous reset signal which resets all FSMs and registers in the core to the default state and values after each frame of encoding.

<b>Signal</b>	<b>Direction</b>	<b>Data width</b>	<b>Description</b>
i_code_len	IN	WL	This is WL bit width input. It mentions about the length of the code of encoded data symbols. All the code lengths defined in the DVB-S2 and DVB-S standard are supported.
i_data_len	IN	WL	This is WL bit input. It mentions about the length of the data symbols to be encoded. All the code lengths defined in the DVB-S2 and DVB-S standard are supported.
i_blk_in_start	IN	1	This is a single bit input port. This signal indicates the starting of input received data block.
i_message	IN	WL	This is input port of <b>WL</b> data width through which data symbols to be encoded will be sent through.
o_encoded_data	OUT	WL	This is the output port of <b>WL</b> width through which encoded data will be given out as output.
o_blk_out_start	OUT	1	This is single bit output port through which a signal is enabled high as long as the output port gives out encoded data. This signal tells the start of the encoded data.
o_blk_out_end	OUT	1	This is single bit port through which a signal is enabled to indicate the ending of the encoded data.
o_ready	OUT	1	This is one bit output signal, which will be enabled after all FSMs, flip-flops and counters have been reseted with synchronous reset signal. Once it is enabled, user could send input frame data to the core.

Table 2: BCH Encoder signal definition table.

### Performance:

<b>Device</b>	<b>Slice Count</b>	<b>Frequency (MHz)</b>
Virtex-4	146	280
Virtex-5	78	285

Table 3: BCH Encoder Core performance table.

### Verification:

The BCH Encoder core module has been verified with following approaches:

- Exhaustive Functional/Timing simulation.
- Results compared with MATLAB functions and C source code functionality.

The BCH Encoder core has been tested for the following industry standard test cases (N, K).

S. No	N	K
1	15	9
2	31	26
3	63	57
4	127	120
5	182	172
6	204	188
7	208	192
8	255	239
9	255	233
10	511	502

Table 4: Common N, K values.

#### Deliverables:

- Verilog RTL source code
- The IP core test environment developed in verilog HDL (test benches).
- Synthesis and Simulation scripts.
- Detailed user documentation, including RTL source code documentation.
- Architecture specification.

#### Applications:

Typical application of BCH encoder is in DVB standard. It is used for Forward Error Correction (FEC) in communication systems where data transmitted through channels is subjected to errors and erasures.

The field used is GF(256). The standard encoder is BCH(204, 188). GF(256) is used in many applications, because each of the 256 field elements can be represented as on 8 bit sequence or byte. BCH codes of length 255 are thus very popular error correction codes. Various BCH encoder applications include:

1. Deep space telecommunications.
2. Hard drive or disk controller applications.
3. Computational storage system applications.
4. CD or DVD controller applications.
5. Fiber optic systems. Currently RS (255, 239) code is commonly used in high speed fiber optic systems.
6. Wireless communication systems.
7. DTV/HDTV broadcast.
8. ADSL, xDSL.
9. Cellular telephone systems.
10. Micro wave link systems.
11. Satellite communications, digital television systems.