

Data sheet for Binary BCH Decoder Core

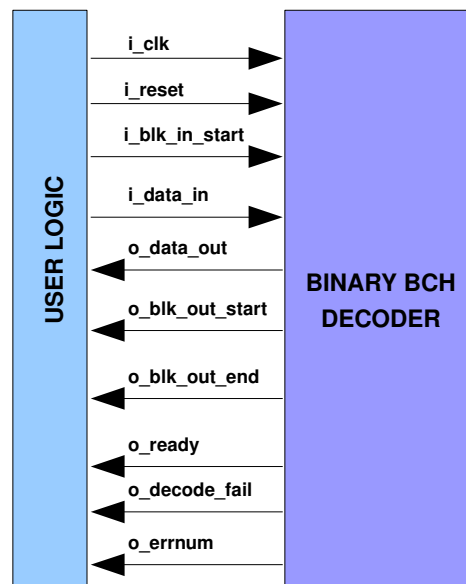
Functional Description:

Binary BCH codes form a large class of powerful random error correcting cyclic codes. These codes occupy a prominent place in theory and practice of error correction. Softjin's Binary BCH decoder core provides the user an easy way to configure the BCH decoder core to suit his application requirements

Features:

- High speed Binary BCH decoding algorithm.
- Fully Synchronous design.
- Core can be compile time configured for any value of code length 'N' and data length 'K'
- Easy user interface

Block Diagram:



Binary BCH Decoder Parameter Table

This table describes the general Binary BCH Decoder parameters:

<i>Parameter</i>	<i>Description</i>
CODE_LENGTH(N)	Represents length of the codeword
MSG_LENGTH(K)	Represents length information word
NUM_COR_ERROR(T)	Represents the maximum number of correctable errors
GF_SIZE(M)	Represents the finite field size

Table 1: Binary BCH Decoder Parameter table.

Pin description table:

<i>Port</i>	<i>Direction</i>	<i>width</i>	<i>Description</i>
i_clk	Input	1	Host clock input
i_reset	Input	1	Active high synchronous reset
i_data_in	Input	1	Encoded data bit input
i_blk_in_start	Input	1	Input pulse applied to indicate start of encoded data bits

<i>Port</i>	<i>Direction</i>	<i>width</i>	<i>Description</i>
o_data_out	Output	1	Corrected data output
o_blk_out_start	Output	1	Output valid signal for the corrected data bits
o_blk_out_end	Output	1	Output pulse to indicate the completion of a block
o_decode_fail	Output	1	Asserted high when decoder failed to correct the errors. It happens when the number of errors occurred are more than the maximum number of correctable errors
o_ready	Output	1	Asserted high when decoder is ready to accept the encoded data
o_errNum	Output	$\log_2(T)$	Indicates the number of errors found

Table 2: Binary BCH Decoder Pin description table.

Performance:

Configuration (N, K)	Device	Slice DFFs	Slice LUTs	Frequency (MHz)	Throughput @100Mhz for 'K' information bits	
(127, 22)	Virtex-5	2471	2831	385	Erroneous case	1.6 Mb/s
					Non erroneous case	8.5 Mb/s
(127, 8)	Virtex-5	3227	3712	290	Erroneous case	512 Kb/s
					Non erroneous case	3 Mb/s

Table 3: Binary BCH Decoder Core performance table.

Verification:

The Binary BCH Decoder core module has been verified with following approaches:

- Exhaustive Functional/Timing simulation for numerous BCH combinations
- Results compared with MATLAB functions.
- On Board verification on a custom board with Xilinx's Spartan 3A-DSP FPGA on it.

Deliverable:

- Verilog RTL source code
- Verilog test bench for design validation
- Detailed design documentation, including RTL source code documentation.

Applications :

Binary BCH decoder typical applications include:

- Deep space telecommunications.
- Hard drive or disk controller applications.
- ECC module in NAND flash controllers.
- Wireless communication systems.
- Cellular telephone systems.
- Micro wave link systems.
- Satellite communications, digital television systems