

Data sheet for BCH Decoder Core

Introduction:

BCH codes are mainly used in communication systems requiring Forward Error Correction (FEC) as an error detector and correctors where data transmitted through communication channel is viable to errors and erasures. This can be targeted to both FPGA and ASIC technologies.

During encoding redundant data called *parity symbols* are appended to data symbols to detect and correct errors in the data during decoding. Usually these errors are mainly due to channel noise. The error correcting capability of decoder depends upon number of parity symbols appended to actual data block.

The BCH decoder receives N symbol code word consisting of K symbol data appended with 2T parity symbols. It can detect and correct up to T possible symbol errors or up to 2T symbol erasure symbol errors, where T is $(N-K)/2$. When number of errors presented in code word exceeds T, then decode failure occurs.

Functional Description:

The BCH decoder has five main functional blocks along with memory blocks. Syndrome calculation block calculates syndrome components which tell about presence of errors in the encoded data. Error

locator polynomial block computes error locator polynomial whose inverse of roots gives error locations. A polynomial solver in error location unit solves this error locator polynomial and gives error locations. Error magnitudes block computes error magnitudes. Decoding block decodes received encoded data with error magnitudes and strips of parity symbols and finally gives out decoded output.

Features:

- High speed BCH decoding algorithm.
- Fully compliant with standard such as DVB-s2 and DVB-S standards.
- Compatible with all code and data lengths.
- It supports both error and erasure decoding.
- Synchronous design.
- Provision to change code rates dynamically.
- Available for Xilinx FPGA and ASIC implementation.
- Core can be configured for any value of code and data lengths N and K
- Area and power optimized implementation
- Compatible, flexible and easy integration with other modules.

Block Diagram:

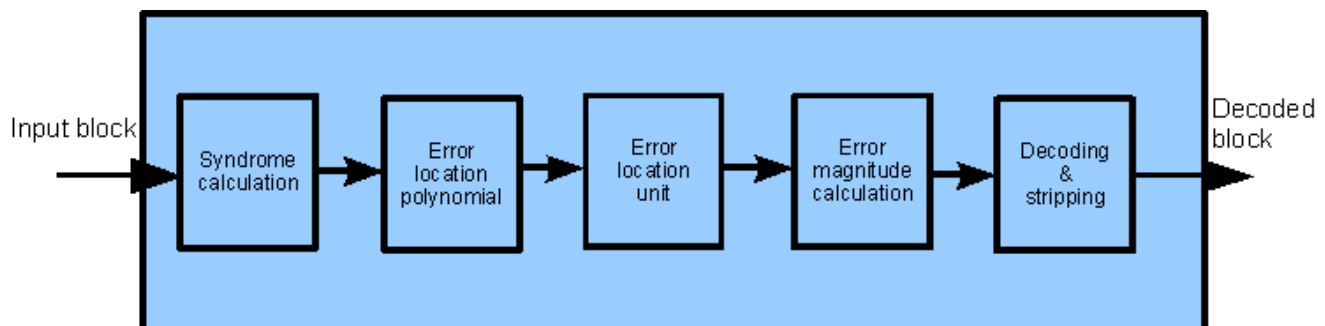


Figure 1: BCH Decoder Block Diagram

Parameters:

This table describes the general BCH Decoder parameters:

Parameter	Type	Description
WL	Integer	Represents width of the each data symbol.

Table 1: BCH Decoder Parameter table.

Schematic Symbol

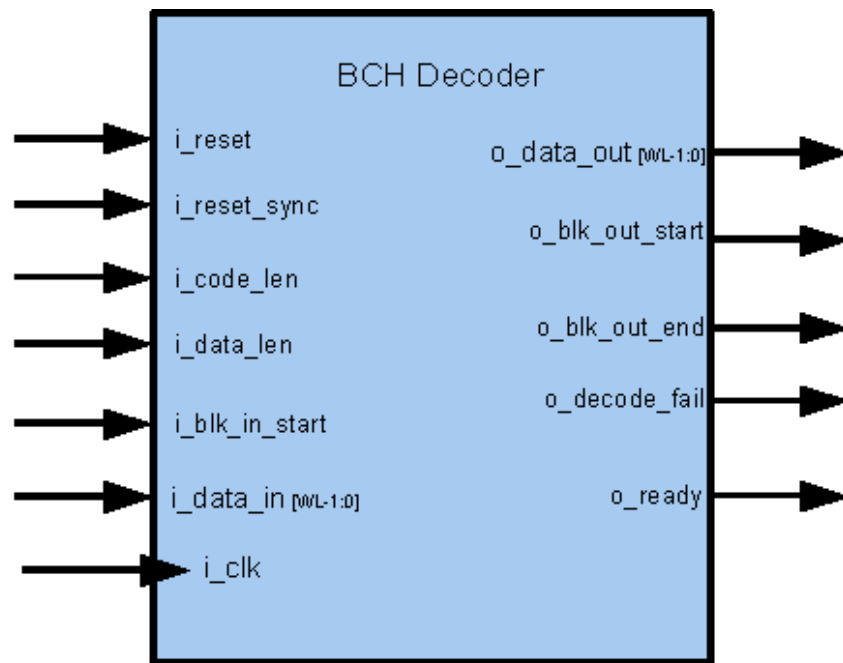


Figure 2: BCH Decoder Schematic Diagram

Signal Definition:

Signal	Direction	Data width	Description
i_clk	IN	1	This BCH Decoder is single clock system and all I/Os and internal decoder processor is in synchronous with it.
i_reset	IN	1	This signal resets the system whenever it is enabled and all counters, registers are sets to starting point.
i_reset_sync	IN	1	This is synchronous reset signal which resets all FSMs and registers in the core to the default state and values after each frame of encoding.
i_data_in	IN	WL	This is input port of WL data width through which pixel data is fed through.

Signal	Direction	Data width	Description
i_code_len	IN	1	This is WL bit width input. It mentions about the length of the code of input encoded data symbols. All the code lengths defined in the DVB-S2 and DVB-S standard are supported.
i_data_len	IN	1	This is WL bit input. It mentions about the length of the decoded data symbols. All the code lengths defined in the DVB-S2 and DVB-S standard are supported.
i_blk_in_start	IN	1	This signal indicates the starting of input received data block. As long as this signal is high, indicates that data presented at input port i_data_in is valid received block data.
o_data_out	OUT	WL	This is the port through which decoded received input data will be given out as output.
o_blk_out_start	OUT	1	This signal gives information about starting point of decoded output block.
o_blk_out_end	OUT	1	This signal gives information about ending point of decoded output block.
o_decode_fail	OUT	1	This is single bit output port. When number of errors presented in the input of the decoder, this signal will be enabled and then core is ready to take up next input frame.
o_ready	OUT	1	This is one bit output signal, which will be enabled after all FSMs, flip-flops and counters have been reseted with synchronous reset signal. Once it is enabled, user could send input frame data to the core.

Table 2: BCH Decoder signal definition table.

Performance:

Device	Slice Count	Frequency (MHz)
Virtex-4	776	253
Virtex-5	373	300

Table 3: BCH Decoder Core performance table.

Verification:

The BCH Decoder core module has been verified with following approaches:

- Exhaustive Functional/Timing simulation.
- Results compared with MATLAB functions and BCH Decoder -C code functionality.

The BCH Encoder core has been tested for the following industry standard test cases (N, K). These N, K values are sent to BCH Decoder core through input ports **i_code_len** and **i_data_len**.

No	N	K
1	15	9
2	31	26
3	63	57
4	127	120
5	182	172
6	204	188
7	208	192
8	255	239
9	255	233
10	511	502

Table 4: Common N, K values

Deliverables:

- Verilog RTL source code
- The IP core test environment developed in verilog HDL (test benches).
- Synthesis and Simulation scripts.
- Detailed user documentation, including RTL source code documentation.
- Architecture specification.

Applications:

Typical application of BCH decoder is in DVB standard. It is used for Forward Error Correction (FEC) in communication systems where data transmitted through channels is subjected to errors and erasures.

The field used is GF(256). The standard decoder is RS(204, 188). GF(256) is used in many applications, because each of the 256 field elements can be represented as on 8 bit sequence or byte. RS codes of length 255 are thus very popular error correction codes. Various BCH decoder applications include:

1. Deep space telecommunications.
2. Hard drive or disk controller applications.
3. Computational storage system applications.
4. CD or DVD controller applications.

5. Fiber optic systems. Currently RS (255, 239) code is commonly used in high speed fiber optic systems.
6. Wireless communication systems.
7. Cellular telephone systems.
8. Micro wave link systems.
9. Satellite communications, digital television systems