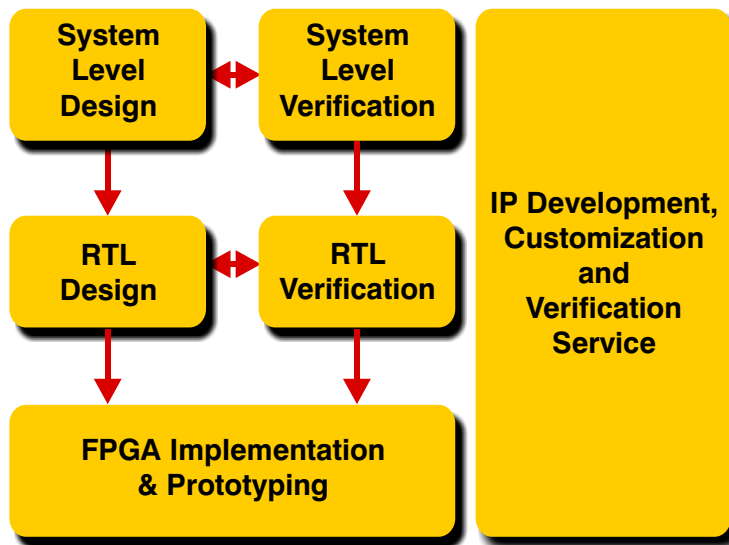


SoftJin's Hardware Design Service



SoftJin hardware design and verification service solution includes

- Algorithm development for high performance applications
- System Level Architecture Optimizing
- HW-SW partitioning
- RTL modelling using Verilog, VHDL
- Use of platform FPGAs, embedded processors, memories, controllers
- Synthesis, simulation, physical design, timing closure for FPGA platform
- Test bench development, coverage analysis, synthesizable test bench development etc.

SoftJin offers hardware design and verification service across the complete value chain of Microprocessor/ FPGA based hardware design starting from System design to bit-stream generation. We also provide the design and verification service for ASIC based design except the physical design and layout.

System Level Design Service

- Design, analysis and optimizations of algorithms for enabling high performance
- Virtual prototyping and architecture exploration of systems using SystemC, C/C++ modelling at various level of abstraction – Architecture level (both timed and untimed functional modes), Transaction level, Behavioural hardware level, Register-transfer (RT) level
- Hardware-Software Partitioning
- Analysis of performance, cost, risk trade-offs at System Level
- Model conversion from HDL to C/C++, SystemC

RTL Design Service

- Block and Sub-system level partitioning of design
- RTL modeling using various hardware description languages like System Verilog, Verilog, VHDL etc.
- Evaluation, customization and integration of third party IPs

System and RTL Verification

- Preparation of System Verification Plan
- Design and implementation of System Simulation Environment
 - a. Test bench development using SystemC, System Verilog, C/C++, HDLs and scripting languages such as Perl, Tcl/Tk
 - b. Perform coverage analysis
- Hardware-Software co-simulation and co-verification
- Assertion based verification

- Constraint random generation approach to get maximum verification coverage
- Use of Synthesizable test-benches for faster verification on FPGA based hardware accelerator
- Development of re-usable Verification IPs like Bus Functional Model etc.
- Third Party IP verification
- Expertise in verification of designs using cores like ARM, PowerPC and Interfaces such as PCI-express, I2C, GbE, AHB etc.

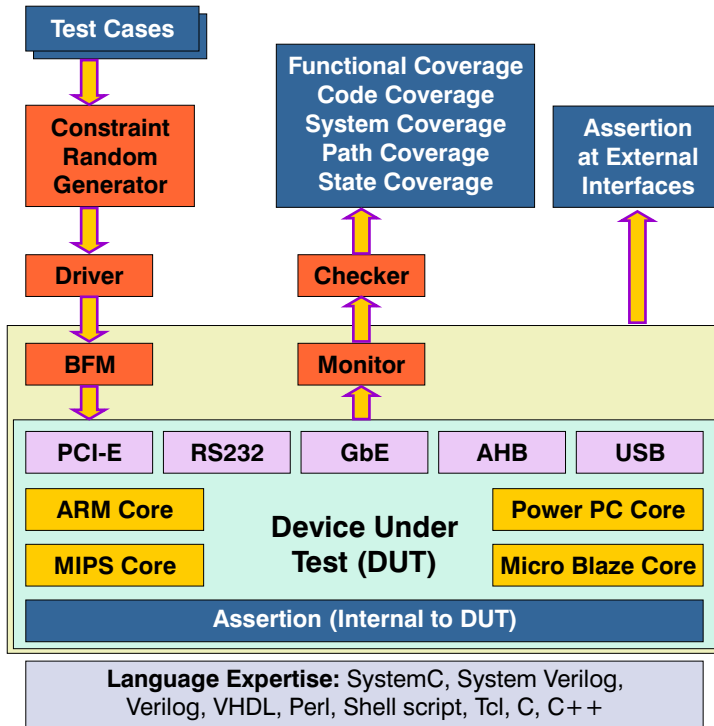
High Performance FPGA based System

- Expertise in use of Platform FPGA devices with embedded processors (Microblaze, NIOSII etc.), memories, interfaces and dedicated data-path elements
- Multi-FPGA design partitioning, implementation and verification
- Expertise in use of industry standard FPGA Synthesis, Simulation, Equivalence Checking, Floor-planning, P&R and Timing analysis tools
- Making best use of available special resources in the FPGA/Programmable Platform such as Processors, Memories, Interfaces and dedicated data-path elements
- Experience in handling complex, high-speed and high-density designs

IP Development, Customization and Verification Service

- Development of new IP complying to a industry standard or customer's specifications
- IP development at various levels of abstraction including C/C++, RTL level
- Customization of SoftJin authored or third party IP for specific FPGA and other Programmable platforms
- Migration of IP from one platform to another
- Verification of existing IP for functional correctness and performance benchmarking
- Evaluation and benchmarking of IP

SoftJin's Verification Skills



SoftJin's prior experience in Application and IP Design Service

DSP Functions: FFT/ IFFT, FIR, IIR, DCT/ IDCT

I/O Interface: USB cntl., I2C cntl., LCD cntl.

Memory Cntl.: SSRAM cntl., SDRAM cntl., EEPROM cntl.

Communication IPs: Bloom Filter, Checksum Calculator, Hamming Code recv/ transmitter, Cryptographic hash func.

Communication Application: Ingress Packet Processing for specific telecom protocol (combined header parser, scheduler, queue manager, packet editor)

Image Processing Application: Edge-detection, histograms, image scaling, image arithmetic

Other Application: Data Encryption, High Speed Data

SoftJin is a Bangalore based company focused on product and service for Electronic Design Automation as well as system design and verification areas.

Our key customers include:

- Innovative Programmable Fabric Companies
- IDMs requiring custom EDA tools
- EDA Product companies
- Semiconductor manufacturers – Mask shops, Foundries and Semiconductor Equipment makers

For more information please contact sales@softjin.com

Case Study 1: Multi-FPGA based System Design for high speed Production Environment

SoftJin's Contribution

- ▶ Realization of hardware using multiple FPGAs. Multiple memories used as buffers for each stage of macro-pipeline FPGA system.
- ▶ Integration of FPGA devices with Board
- ▶ Achieved desired overall throughput of the system data driven to lithography equipment at 1 GigaBytes/sec

The key FPGA design related skills used in these projects are

System level design

- ▶ Hardware-Software Partitioning
- ▶ Hardware-Software Co-Verification using SystemC
- ▶ Multi-FPGA Partitioning

FPGA Implementation

- ▶ RTL modeling using Verilog, VHDL
- ▶ Platform FPGA design using Xilinx Virtex Pro
- ▶ Usage of standard design elements including DDR SDRAM memory controller, Bus Controller
- ▶ Tools used Synplify Pro, Xilinx XST,
- ▶ ModelSim with SystemC

Verification Techniques

- ▶ Proprietary verification strategy using re-usable SystemC testbenches
- ▶ Synthesizable test-bench to allow on-chip verification of RTL module

Case Study 2: Acceleration of Snort based Network Intrusion Detection System

- ▶ Microblaze based multi-core FPGA architecture using Virtex-4
- ▶ Snort consist of 3000+ rules
- ▶ Each packet Header and Payload is inspected for specific signatures
- ▶ Porting Snort on multi-core architecture can give significant increase in throughput
 - Split Snort rule-set into multiple partition
 - Each processor-core works on the partitioned smaller rule-set

SoftJin

Enabling Electronic Design

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