

FPGA Routing Engine

High performance Timing Driven Routing Engine for Island style FPGAs

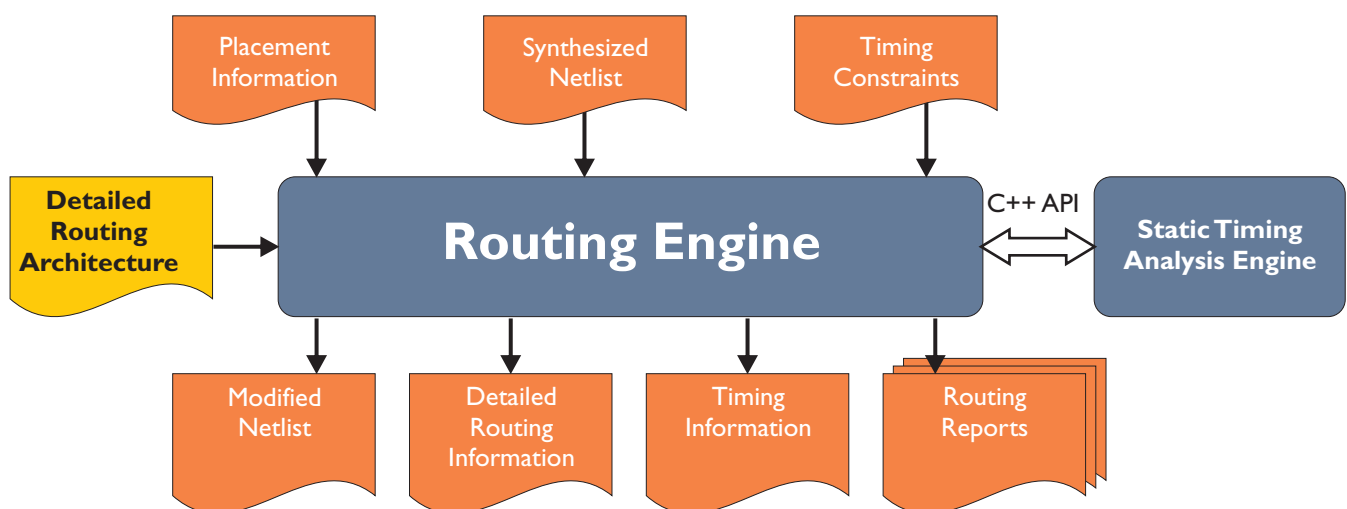
SoftJin's FPGA Routing Engine is a Timing driven Routing Engine for island based FPGA architectures. It is a fast, cross-platform Router that meets the timing goals, while optimizing the use of Routing Resources of the FPGA. SoftJin's Routing Engine is a core EDA component that can be used by FPGA vendors to offer a customized, best-in-class Routing Engine as part of their tool suite to the FPGA users. It is available on both, Windows and Linux platforms.

The Routing Engine has been designed to support the following FPGA architecture:

- Homogeneous logic blocks
- Island type architecture with logic blocks embedded in a sea-of-interconnects
- Cluster based organization of functional/logic elements in a logic block
- Non-hierarchical interconnect structure
- Segmented routing architecture with switch boxes

Key Benefits for FPGA vendors

- **Hit the market faster with a customized Routing Solution -** As compared to developing the Routing Engine in-house from scratch, SoftJin's Routing Engine enables you to hit the market much faster with a Routing Solution customized and performance tuned for your device architecture.
- **Lower cost of ownership -** A combination of SoftJin's FPGA Routing Engine licensing and customization service offers much lesser cost of ownership as compared to developing and supporting such a solution in-house.



Key Features

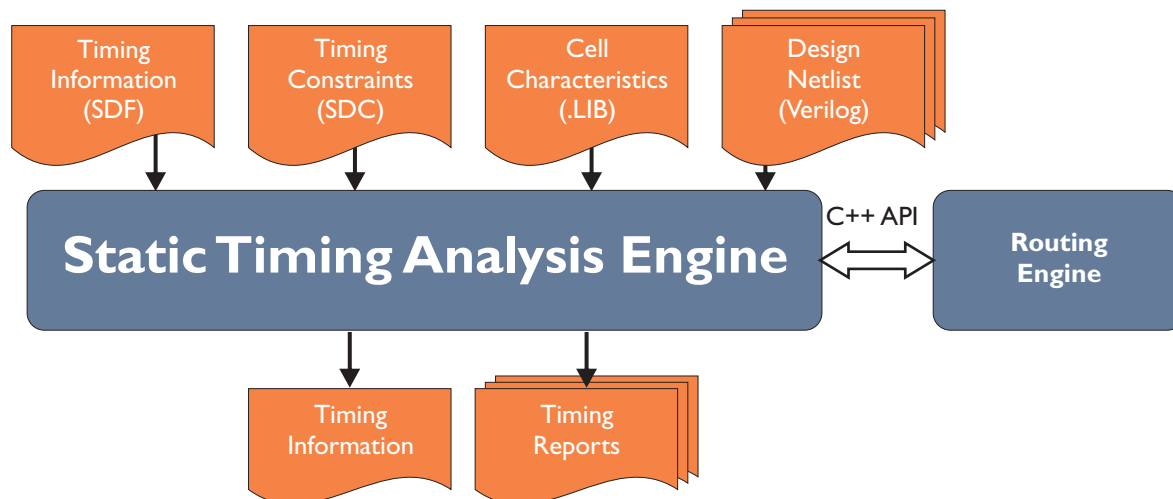
- **Timing driven** - The routed circuit meets the timing constraints and at the same time minimizes the congestion
- **Well Defined Interfaces** to easily integrate into the design flow
- Reads the Routing Architecture, Placement Information, Synthesized Netlist information and the Timing constraints using well-defined Interfaces.
- Writes the Routing Information, modified Netlist and the Timing Information using well defined interfaces.
- Generates **Rich routing reports** with statistics about the Routed design.
- **Allows permutations** of logically equivalent input pins of logic block in order to reduce congestion and optimize timing.
- **Interfaces with SoftJin's Static Timing Analysis Engine** through a well defined interface. Can also be integrated with other third party STA Engine.
- Accepts **various control parameters** to control the Run-time behavior of the Router.

SoftJin offers **Router customization and integration services**, whereby SoftJin takes the responsibility of customizing and tuning the Routing Engine for specific device architecture and integrating the Router with the other tools in the flow.

Static Timing Analysis Engine

EDA building block for supporting Timing Optimization in EDA tools

SoftJin's Static Timing Analysis Engine is an EDA building block that can be integrated to run in close loop with EDA tools involving timing optimization such as Synthesis, Placement and Routing tools. Originally designed and integrated with SoftJin's FPGA Routing Engine, SoftJin's STA engine is available as an object library with well defined interfaces for integration with other EDA tools. It is available on both, Windows and Linux platforms.



Key Features

The STA Engine has the following key features:

- The STA Engine has the capability to carry out timing analysis on the input netlist using cell delays available through .lib and net delays available through SDF or through appropriate annotation API. The Engine computes slack values for all nets in the design and returns those through API calls.
- The engine can carry out the timing analysis for both **setup** (max-analysis) and **hold** (min-analysis) violations.
- The Engine finds out **k most critical paths** and also reports maximum frequency
- Supports sub-set of SDC constraints including **false path**, multi-cycle path specification, max/min delay constraints
- Support for **incremental timing analysis** due to Netlist change or change in net delay
- Handles circuits with **multiple clocks and generated clocks**

- **Well Defined Interfaces** to easily integrate into the design flow - The STA Engine accepts the delay information, delay constraints, cell characteristics and the design net-list in standard formats. Similarly, the STA Engine generates delay information in SDF format along with the Timing Report
- The STA Engine interfaces with SoftJin's Routing Engine through a well defined C++ API interface. Similarly, the STA Engine can be integrated with any other third party Routing, Placement or Synthesis Engine

SoftJin offers **STA customization and integration services**, whereby SoftJin takes the responsibility of customizing the STA Engine for specific requirements of the customer and integrating the STA engine with the other tools in the flow.

To know more about the above and other EDA Building Blocks for Programmable Platforms like Programmable Synthesis Engine, please contact sales@softjin.com

SoftJin

Enabling Electronic Design

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